General Description

The TP292X is a high performance 8-bit RISC-based microcontroller with on-chip 2×1K bytes or one 4K bytes One Time Programmable (OTP) memory. Oscillator frequency can be as high as 10 MHz. The device features an on-chip oscillator, a single-cycle CPU core, RAM, one-time-programmable memory, 24-bit multifunctional I/O ports, and the following on-chip peripherals: 10-bit 200 SPS analog-to-digital converter, 3 sets of analog comparators, and built-in two 10 bit multipurpose Timers/PWM, and one 8 bit multipurpose timer for period mode.

The TP292X is designed for a wide range of applications, ranging from industrial control, consumer products, household appliances control subsystem, to low-power remote sensor. The small footprint packages make the device perfect for all applications with space limitation. Low-cost, low-power, high-performance, ease of use and I/O flexibility make the TP292X very versatile.

Features

CPU Features

- A single cycle 8-bit RISC MCU with oscillator frequency 8 MHz in standard, and as high as 10 MHz
- More than 100 instructions with immediate, direct, in-direct addressing and long, short, indirect jump supported
- Support versatile conditional branch, and skip instructions
- 32 bytes general purpose register
- 16 bit stack pointer
- Operation Voltage 3V ~ 5.5V

Memory Features

- Configurable program memory with one consecutive 2K word (4 K bytes) OTP or with two 1K words memory space
- Support 256 byte data SRAM

Reset Features

- Support 4 types of reset; pin reset, power-on reset (POR), low-voltage reset (LVR), and watchdog timer reset

Oscillator and Clock Generator Features

- Support 3 types of oscillator mode
  - Internal high speed RC oscillator mode: 8 MHz (calibrated), and need no external components
  - Internal low speed RC oscillator mode: 128 KHz, and need no external components
  - External clock through I/O ports
- Support 3 types of sleep mode; IDLE and POWER-DOWN

Timer and PWM Features

- Two 10 bit timers for period, PWM, and ICP mode
- One 8 bit timer for period mode

I/O Features

- 24 bit multifunctional, bi-directional I/O, each bit with selective interrupt and wakeup sleep
  - Port A: 8 bit I/O, shared with timer0/PWM
  - Port B: 8 bit I/O, shared with timer1/PWM, and analog comparator
  - Port C: 4 bit I/O, shared with timer0～3, and ADC input-pin 0～3
  - Port D: 4 bit I/O, shared with fast crystal, and system clock in/out

Analog Comparator (ACMP) Features

- 3 independent ACMP with selectable interrupt

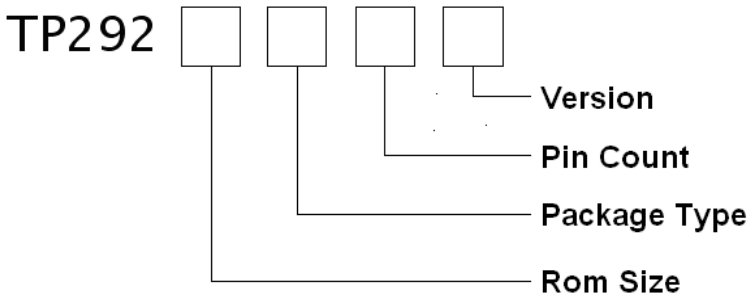
Analog to Digital Converter (ADC) Features

- 10 bit resolution with up to 200K SPS

Package Forms

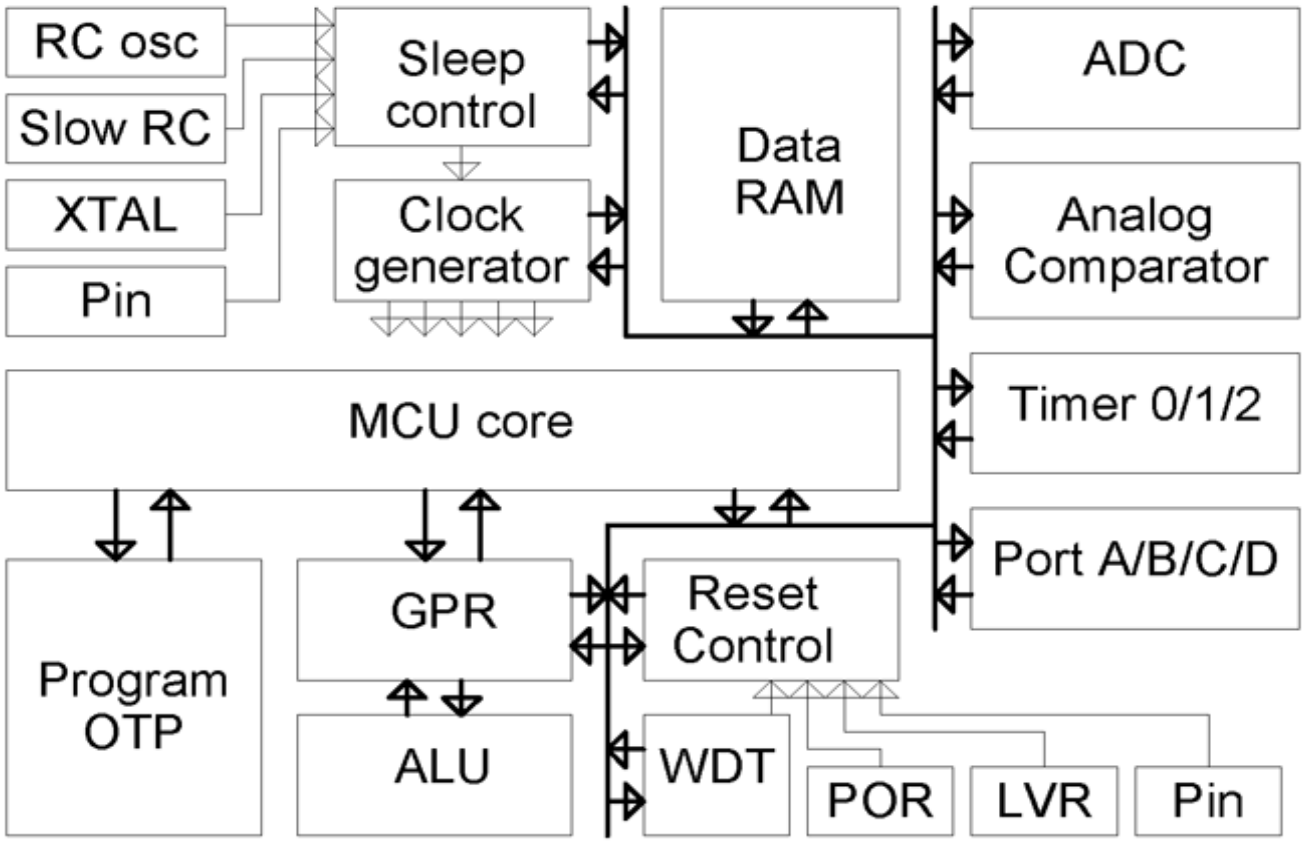
- SSOP/ SOP/ PDIP 16/20/28 pins

Ordering Information



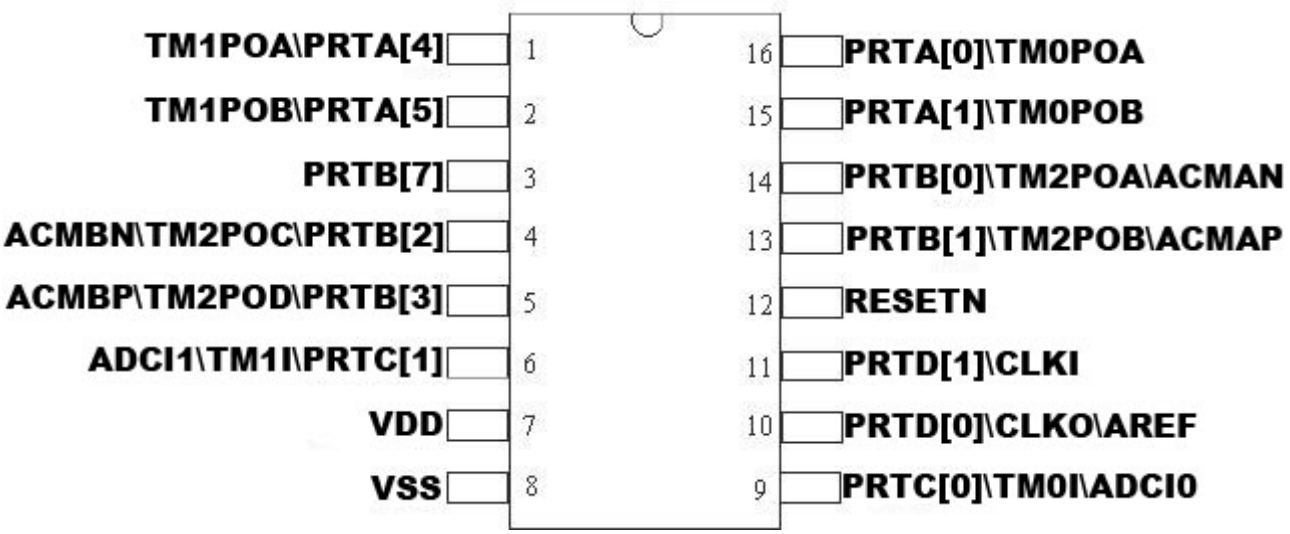
Rom Size	2 : 4K
	1 : 2K*2
	0 : 2K
Package Type	P : PDIP
	M : SOP
	Z : SSOP
Pin Count	16
	20
	28

Block Diagram



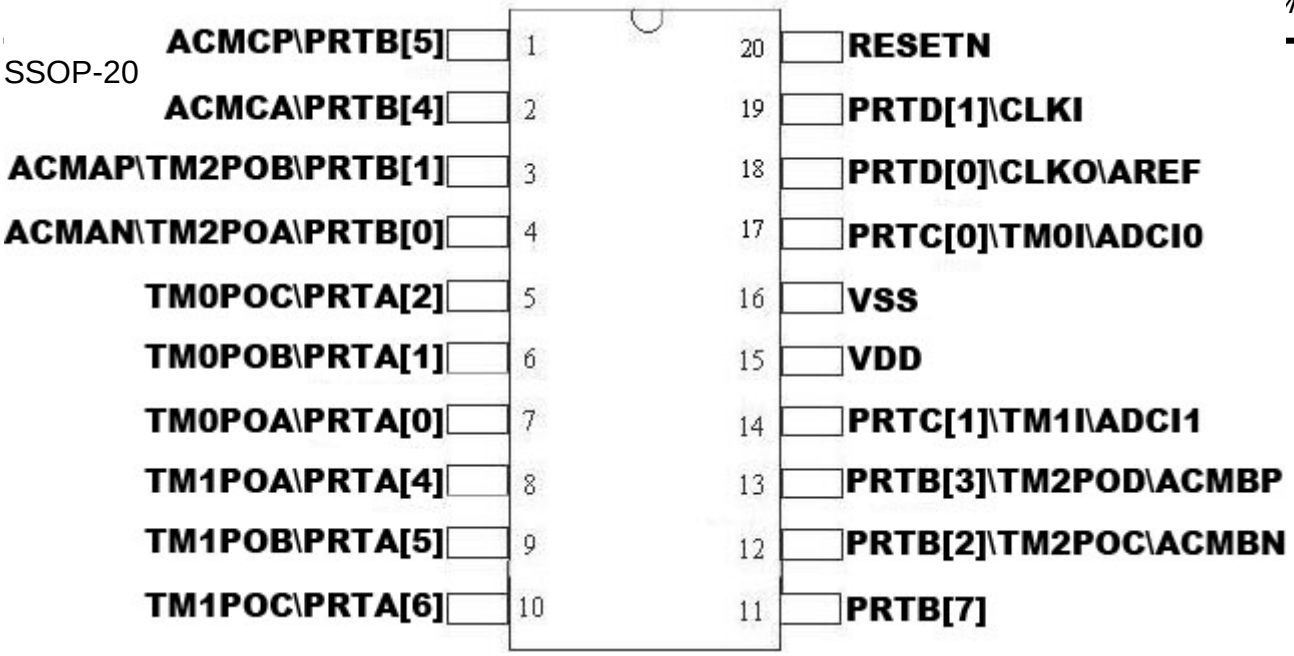
Pin Configuration

SSOP-16



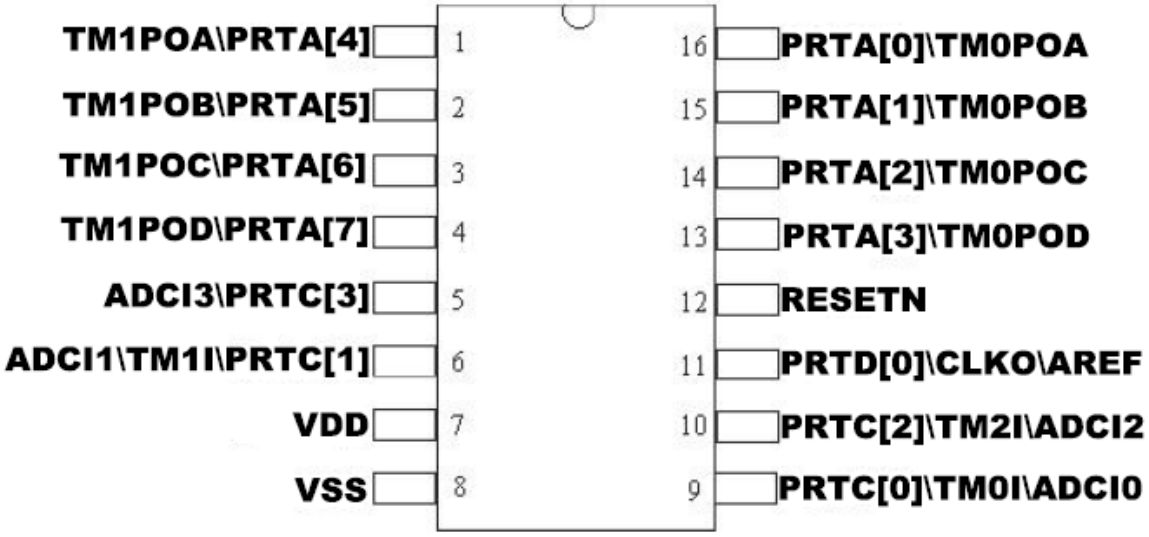
Pin #	Pin Name	Description
1	PRTA[4]	Port A bit 4, Timer 1 PWM output
2	PRTA[5]	Port A bit 5, Timer 1 PWM output
3	PRTB[7]	Port B bit 7
4	PRTB[2]	Port B bit 2, ACMP B negative input
5	PRTB[3]	Port B bit 3, ACMP B positive input
6	PRTC[1]	Port C bit 1, Timer 1 input, ADC input 1
7	VDD	Positive power
8	VSS	Ground
9	PRTC[0]	Port C bit 0, Timer 0 input, ADC input 0
10	PRTD[0]	Port D bit 0, CPU clock output, ADC external reference voltage
11	PRTD[1]	Port D bit 1, external clock input
12	RESETN	Reset
13	PRTB[1]	Port B bit 1, ACMP A positive input
14	PRTB[0]	Port B bit 0, ACMP A negative input
15	PRTA[1]	Port A bit 1, Timer 0 PWM output
16	PRTA[0]	Port A bit 0, Timer 0 PWM output

SSOP-20



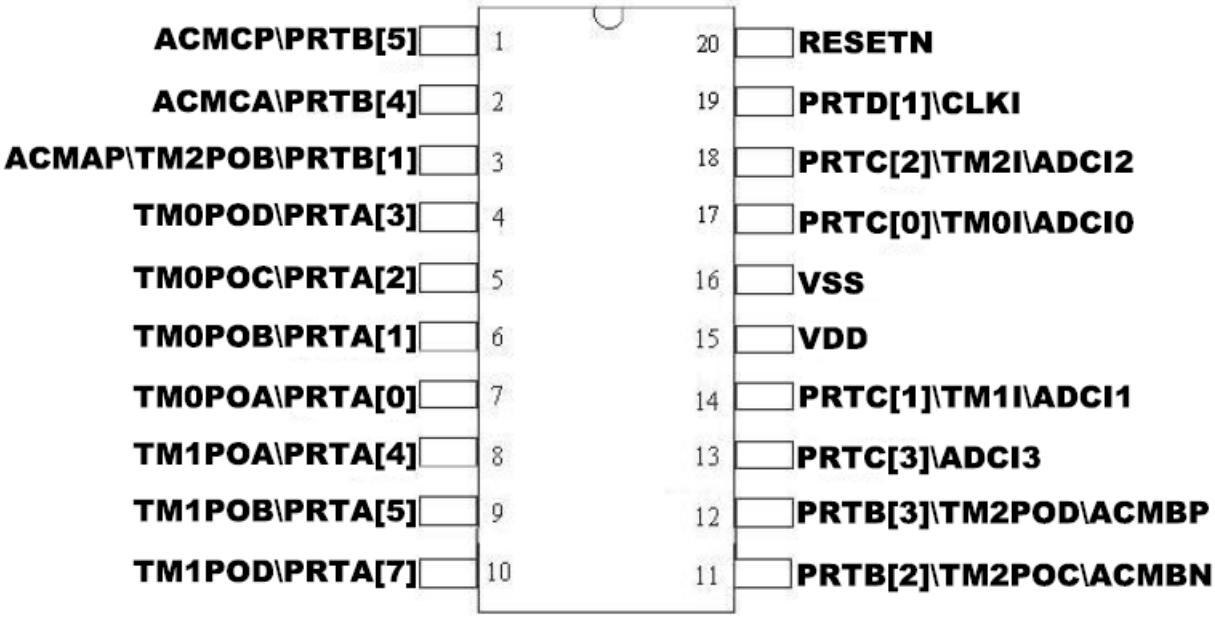
Pin #	Pin Name	Description
1	PRTB[5]	Port B bit 5, ACMP C positive input
2	PRTB[4]	Port B bit 4, ACMP C negative input
3	PRTB[1]	Port B bit 1, ACMP A positive input
4	PRTB[0]	Port B bit 0, ACMP A negative input
5	PRTA[2]	Port A bit 2, Timer 0 PWM output
6	PRTA[1]	Port A bit 1, Timer 0 PWM output
7	PRTA[0]	Port A bit 0, Timer 0 PWM output
8	PRTA[4]	Port A bit 4, Timer 1 PWM output
9	PRTA[5]	Port A bit 5, Timer 1 PWM output
10	PRTA[6]	Port A bit 6, Timer 1 PWM output
11	PRTB[7]	Port B bit 7
12	PRTB[2]	Port B bit 2, ACMP B negative input
13	PRTB[3]	Port B bit 3, ACMP B positive input
14	PRTC[1]	Port C bit 1, Timer 1 input, ADC input 1
15	VDD	Positive power
16	VSS	Ground
17	PRTC[0]	Port C bit 0, Timer 0 input, ADC input 0
18	PRTD[0]	Port D bit 0, CPU clock output, ADC external reference voltage
19	PRTD[1]	Port D bit 1, external clock input
20	RESETN	Reset

SSOP-16 (4 ch ADC)



Pin #	Pin Name	Description
1	PRTA[4]	Port A bit 4, Timer 1 PWM output
2	PRTA[5]	Port A bit 5, Timer 1 PWM output
3	PRTA[6]	Port A bit 6, Timer 1 PWM output
4	PRTA[7]	Port A bit 7, Timer 1 PWM output
5	PRTC[3]	Port C bit 3, ADC input 3
6	PRTC[1]	Port C bit 1, Timer 1 input, ADC input 1
7	VDD	Positive power
8	VSS	Ground
9	PRTC[0]	Port C bit 0, Timer 0 input, ADC input 0
10	PRTC[2]	Port C bit 2, Timer 2 input, ADC input 2
11	PRTD[0]	Port D bit 0, CPU clock output, ADC external reference voltage
12	RESETN	Reset
13	PRTA[3]	Port A bit 3, Timer 0 PWM output
14	PRTA[2]	Port A bit 2, Timer 0 PWM output
15	PRTA[1]	Port A bit 1, Timer 0 PWM output
16	PRTA[0]	Port A bit 0, Timer 0 PWM output

SSOP-20 (4 ch ADC)



Pin #	Pin Name	Description
1	PRTB[5]	Port B bit 5, ACMP C positive input
2	PRTB[4]	Port B bit 4, ACMP C negative input
3	PRTB[1]	Port B bit 1, ACMP A positive input
4	PRTA[3]	Port A bit 3, Timer 0 PWM output
5	PRTA[2]	Port A bit 2, Timer 0 PWM output
6	PRTA[1]	Port A bit 1, Timer 0 PWM output
7	PRTA[0]	Port A bit 0, Timer 0 PWM output
8	PRTA[4]	Port A bit 4, Timer 1 PWM output
9	PRTA[5]	Port A bit 5, Timer 1 PWM output
10	PRTA[7]	Port A bit 7, Timer 1 PWM output
11	PRTB[2]	Port B bit 2, ACMP B negative input
12	PRTB[3]	Port B bit 3, ACMP B positive input
13	PRTC[3]	Port C bit 3, ADC input 3
14	PRTC[1]	Port C bit 1, Timer 1 input, ADC input 1
15	VDD	Positive power
16	VSS	Ground
17	PRTC[0]	Port C bit 0, Timer 0 input, ADC input 0
18	PRTC[2]	Port C bit 2, Timer 2 input, ADC input 2
19	PRTD[1]	Port D bit 1, external clock input
20	RESETN	Reset

Functional Description

The TP292X is a modified Harvard architecture 8-bit high performance RISC microcontroller (MCU). The device is capable of executing more than 100 instructions and features of complete set of addressing mode, I/O flexibility, power-saving mode, PWM capability, and 10-bit resolution ADC. The device can address up to 64K words of program space, as well as up to 64K bytes data space.

CPU

The CPU can do ALU instructions in a single machine cycle. The ALU is a general-purpose arithmetic unit. It performs arithmetic and Boolean functions between data in the working register and any register file. The program counter (PC) is a 16-bit register containing the address of the next instruction to be executed by the CPU and it is capable of pointing up to 64K words of program space.

Stack is a special part of the memory that is used to save the contents of PC only. During interrupts and subroutine calls, the return address of PC is stored on the stack, and at the end of subroutines or interrupts, the PC is resorted to its previous value from the stack. The stack is resided in the general data SRAM, and, therefore, the stack size is only limited by the total SRAM size and the usage of the SRAM. The 16-bit stack pointer (SP) is read/write accessible in the I/O space.

Three different addressing modes are provided; immediate, direct, and indirect.

Program Memory

Program memory is used to hold the application program. Program memory is read whenever the CPU performs a fetching instruction. Internally, an instruction is fetched from program memory during every instruction cycle and latched in the fetch register. After a rest has been issued, the CPU starts program execution from location 0000h.

The TP292X contains 2K words (4K bytes) on-chip OTP (One Time Programmable) memory for program storages that hold program instructions. The program memory is addressed by the 16-bit program counter. These 2K words One Time Programmable memory can either be configured one consecutive 4K bytes memory or two 2K bytes memory space.

Address	Description
0x0000	Reset entry
0x0001	Port A transition INT entry
0x0002	Timer0 Period match INT entry
0x0003	Timer0 Duty match or overflow INT entry
0x0004	WDT time-out INT entry
0x0005	Port B transition INT entry
0x0006	Timer1 Period match INT entry
0x0007	Timer1 Duty match or overflow INT entry
0x0008	Analog Comparator transition INT entry
0x0009	Port C transition INT entry
0x000A	Timer2 Period match INT entry
0x000B 0x000C	Reserved
0x000D	ADC complete INT entry
0x000E	Port D transition INT entry
0x000F 0x03FF	User F/W
0x0400 0x07FF	User F/W

Data Memory

Data memory is used for the dynamic data that is generated by the application program and for the STACK. The stack is a portion of memory where the CPU saves his own internal register data for calling a subroutine.

The TP292X contains 256 bytes on-chip SRAM memory for dynamic data storage. The data memory is partitioned into two banks that contain the General Purpose Registers and the Special Function Registers. The general-purpose registers are used to store data and control information for use with specified instructions. On the other hand, the special function registers are used by the CPU and its peripheral modules to control the operation of the devices.

Address Rang	Capacity	Note
0x0000 ~ 0x001F	32 Byte	GPR
0x0020 ~ 0x005F	64 Byte	I/O, dedicated I/O instructions
0x0060 ~ 0x00FF	160 Byte	I/O, data space instructions only
0x0100 ~ 0x01FF	256 Byte	SRAM

Clock and Oscillator

The TP292X can be operated in four different oscillator options, selectable by fuse options.

- Calibrated internal 8MHz oscillator. This clock may be selected by programming the fuse. Once enabled, the oscillator will operate with no external components. The calibrated internal oscillator provide 8MHz clock, and the frequency is nominal values at 5V and 25°C.
- Internal 128 KHz watchdog oscillator. The internal 128 KHz oscillator is a low power oscillator providing a clock of 128 KHz.

External pin input 1K ～16 MHz oscillator from PRTD[1].
Clock and Oscillator Register

CLKPR (System Clock Pre-scalar)

Bit	7	6	5	4	3	2	1	0	CLKPR
0x00_46	CLKPCE	Reserved			CLKPS[3:0]				I/O_0x26
R/W	R/W	R			R/W				
Reset	0	000			1000				

CLKPS : Clock pre-scalar change enable

- Timed sequence to change CLKPS[3:0]
- Write whit CLKPCE = 1 , and all other bits = 0
- Write with CLKPCE = 1 or 0, and CLKPS[3:0] the desired value
- Write of valid CLKPS must be done within 4 machine cycles after the instruction which set CLKPCE to 1.

CLKPS[3:0]: System clock divide factor

0000 : 1
0001 : 2
0010 : 4
0011 : 8
0100 : 16
0101 : 32
0110 : 64
0111 : 128
1000 : 256 (default)
1001 ～ 1111: reserved

PWRR0 (Power Reduction Register 0)

Bit	7	6	5	4	3	2	1	0	PWRR0
0x00_20	CKDPRTD	CKDPRTC	CKDPRTB	CKDPRTA	CKDTM3	CKDTM2	CKDTM1	CKDTM0	I/O_0x00
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	0	

CKDPRT[x] :

1 : turn off Port[x] clock
0 : turn on Port[x] clock

CKDTM[X] :

1 : turn off Timer[x] clock
0 : turn on Timer[x] clock

PWRR1 (Power Reduction Register 1)

Bit	7	6	5	4	3	2	1	0	PWRR1
0x00_21	Reserved						CKDADC	CKDACMP	I/O_0x01
R/W	R						R/W	R/W	
Reset	000000						0	0	

CKD ADC :

1 : turn off ADC I/F clock

0 : turn on ADC I/F clock

CKDACMP :

1 : turn off ACMP I/F clock

0 : turn on ACMP I/F clock

System Control and Reset

The TP292X provides four source of reset

- External rest. Use RESETn pin as an external rest, the MCU is reset when a low level is present o the RESETn pin.
- Power-on reset (POR). The MCU is reset when the supply voltage is below the power-on reset threshold. The on-chip POR circuit holds the chip in reset until VDD has reached a high enough level for proper operation. A maximum rise time for VDD is required.
- Low-voltage reset (LVR). The MCU is reset when the supply voltage is below the LVR threshold. If VDD falls below detection voltage (refer to characteristic table), the low-voltage situation will reset the chip. On any reset (POR, LVR, Watchdog, etc.) the chip will remain in reset until VDD rises above LVR threshold.
- Watchdog reset. The MCU is reset when the watchdog timer period expires and the watchdog is enabled. A watchdog timer is a free-running timer, which can be programmed by user to serve as a system monitor.

During reset, all I/O registers are set to their initial values, and the program starts from address 0000h.

System Control and Reset Register

MSR (MCU Status register)

Bit	7	6	5	4	3	2	1	0	MSR
0x00_54	Reserved				WDRF	LVRF	PINRF	PORF	I/O_0x34
R/W	R				R/W	R/W	R/W	R/W	
Reset	0000				See left	See left	See left	See left	

WDRF :

1 : WDT reset occurs

0 : clear by POR or F/W

LVRF :

1 : LVR reset occurs

0 : clear by POR or F/W

PINRF :

1 : Pin reset occurs

0 : clear by POR or F/W

PORF :

1 : POR reset occurs

0 : clear by or F/W

WDTCSR (WDT Control and Status Register)

Bit	7	6	5	4	3	2	1	0	WDTCSR
0x00_41	WDIF	WDIE	WDCE	WDE	WDP[3:0]				I/O_0x21
R/W	R/W	R/W	R/W	R/W	R/W				
Reset	0	0	0	0	0000				

WDIF : WDT INT flag

1 : flag set

0 : no INT request

WDCE: WDT change enable (see below)

1 : enable change

0 : disable

WDP[3:0]: WDT reset/INT interval

0000 : 2K WDT osc cycles

0001 : 4K

0010 : 8K

WDIE: WDT INT enable (see below)

1 : enable

0 : disable

WDE: WDT enable (see below)

1 : enable

0 : disable

0011 : 16K
0100 : 32K
0101 : 64K
0110 : 128K
0111 : 256K
1000 : 512K
1001 : 1024K
1010 ～ 1111 : reserved

- **WDE and WDIE control function**

WDE	WDIE	WDT	Action
0	0	Stopped	None
0	1	Running	INT
1	0	Running	Reset
1	1	Running	INT

- WDE and WDP update
  - WDE = 0 upon reset
  - Write WDE = 1 without special restriction
  - Change WDP without special restriction
  - To write WDE = 0
    - ✧ Clear WDRF in MSR
    - ✧ Write WDCE = 1 and WDE = 1
    - ✧ Within 4 machine cycles, write WDCE = 0 and WDE = 0

Power Management

The device contains a clock management block that provides the controlling software with a means to dynamically disable/enable the clocks to unused modules in the design thereby saving power, which makes the device an ideal choice for low power applications.

Power Management Register

The TP292X provides 2 sleep modes that allowing the user to tailor the power consumption to the application's requirements. The table shows the different sleep modes. All the sleep modes are either waked-up by I/O ports or by timers.

Mode	OSC	CPU	Timer	I/O	ADC
Normal	Active	Active	Active	Active	Active
Idle	Active	Off	Active	Active	Off
Power down	Off	Off	Off	Off	Off

- Idle mode. By setting SLPE to 1 and SLPM[1:0] to 00 of MCR register, the SLEEP instruction makes the MCU enter idle mode, which stopping CPU and ADC but allowing the oscillator, timer, I/O to continue operating.

Power-down mode. By setting SLPE to 1 and SLPM [1:0] to 10 of MCR register, the SLEEP in instruction makes the MCU enter power down mode. In this mode, the oscillator, CPU, timer, I/O, ADC are all stopped. This mode halts all generated clocks, and exit from this mode is reached by a hardware reset or external interrupts when enabled and set to level triggered Power Management Register

MCR (MCU Control Register)

Bit	7	6	5	4	3	2	1	0	MCR
0x00_55	LVRSLP	PORTUD	SLPE	SLPM[1:0]		LVRSLPE	Reserved		I/O_0x35
R/W	R/W	R/W	R/W	R/W		R/W	R		
Reset	0	0	0	00		0	00		

LVRSLP :

1 : disable LVR during SLEEP

0 : LVR still enable according to fuse LVRLEVEL

PORTUD :

1 : disable all IO port pull-up

0 : enable (according to individual IO port bit register)

SLPE :

1 : enable SLEEP entry

0 : disable

SLPM[1:0] : SLEEP mode selection

00 : Idle

01 : reserved

10 : Power down

11 : Reserved

LVRSLPE : LVR sleep control

1 : start the timed sequence

0 : inhibit LVRSLP from being set

- `1' needs to be written to SLPE before SLEEP instruction in order to enter SLEEP mode.
- A timed sequence initialized by LVRSLPE and LVRSLP is necessary to turn off LVR during SLEEP.
  - Write LVRSLPE = 1 and LVRSLP = 1
  - Within 4 machine cycles after the instruction above, write LVRSLPE = 0 and LVRSLP = 1
  - Within 4 machine cycles after the instruction above, issue SLEEP instruction. Otherwise, H/W will clear LVRSLP to 0.

I/O Ports

Interface with peripherals is conducted via 24 bit multifunctional bi-directional I/O ports. These 24 signals are divided into four ports: Port A, Port B, Port C, and Port D. Port A and Port B contain 8 bit, while Port C and Port D consist of 4 bit. All of these I/O ports can be used for input and output operations. In additional to supporting general input/output functions, each bit can trigger an interrupt and wakeup/sleep to the microcontroller.

All the port pins have alternate function in addition to being general digital I/Os.

[X] = A or B or C or D or E or F, it means Port A, Port B, Port C, Port D, Port E and Port F.

[x] = 0 or 1 or 2 or 3 or 4 or 5 or 6 or 7, it means bit 0 or bit 1 or bit 2 or bit 3 or bit 4 or bit 5 or bit 6 and bit 7 for Port.

	P[X]DO	P[X]DI	P[X]DR	P[X]IM
A	0x3B(I/O_0x1B)	0x39(I/O_0x19)	0x3A(I/O_0x1A)	0x32(I/O_0x12)
B	0x38(I/O_0x18)	0x36(I/O_0x16)	0x37(I/O_0x17)	0x40(I/O_0x20)
C	0x70(I/O_##)	0x71(I/O_##)	0x72(I/O_##)	0x73(I/O_##)
D	0x74(I/O_##)	0x75(I/O_##)	0x76(I/O_##)	0x77(I/O_##)

PS. I/O_## no value.

I/O Ports Register

PS. [X] = A, B, C, D

P[X] DO (Port[X] output data)

Bit	7	6	5	4	3	2	1	0	P[X]DO
0x00_3B	P[X]DO[7:0]								I/O_0x1B
R/W	R/W								
Reset	00000000								

P[X]DO[7:0] :

1 : Port[X] output data

0 : Port[X] pull-up on/off

- When read, it is the P[X] DO register value to be read-back, not pin.

P[X]DI (Port[X] input data)

Bit	7	6	5	4	3	2	1	0	P[X]DI
0x00_39	P[X]DI[7:0]								I/O_0x19
R/W	R								
Reset	xxxxxxxx								

P[X]DI[7:0] : Port[X] input data

- Read the logic value appearing on chip pin.

P[X]DR(Port[X] direction)

Bit	7	6	5	4	3	2	1	0	P[X]DR
0x00_3A	P[X]DR[7:0]								I/O_0x1A
R/W	R/W								
Reset	00000000								

P[X]DR[7:0] : Port[X] direction

1 : output

0 : input

- When P[X] DR[x] is `1' (output, the corresponding P[X] DO[x] bit becomes pull-up on/off control.
- At input mode, port[x] pull-up resister is turned if PUD = 0 and P[X] DO[x] = 1.

P[X]IM (Port[X] INT Mask)

Bit	7	6	5	4	3	2	1	0	PWRR0
0x00_32	P[X]IM[7:0]								I/O_0x12
R/W	R/W								
Reset	00000000								

P[X]IM[7:0] : Port[X] INT mask

1 : enable

0 : disable

- If P[X] IM[x] is `1' , the corresponding Port[X] [x] can trigger an INT upon transition to high or to low.
- P[X] GIF bit is set if any of the enabled Port[X] [x] pin has a transition.
  P[X] GIF bit is automatically cleared by H/W upon INT.
- It is up to F/W to read P[X] DI register and determine which pin(s) trigger the INT.

PORTIF (General port INT flag)

Bit	7	6	5	4	3	2	1	0	PORTIF
0x00_5A	Reserved				PDGIF	PCGIF	PBGIF	PAGIF	I/O_0x3A
R/W	R				R/W	R/W	R/W	R/W	
Reset	0000				0	0	0	0	

PDGIF : Port D collected INT flag

1 : INT set

PCGIF : Port C collected INT flag

1 : INT set

PBGIF : Port B collected INT flag

1 : INT set

PAGIF : Port A collected INT flag

1 : INT set

- P[x] GIF bit is set when either bit of the corresponding P[x] GIF is set.
- Each P[x] GIF has a dedicated INT vector and it is automatically cleared by H/W upon INT.

PORTIE (General port INT enable)

Bit	7	6	5	4	3	2	1	0	PORTIE
0x00_5B	Reserved		Reserved		PDGIE	PCGIE	PBGIE	PAGIE	I/O_0x3B
R/W	R		R		R/W	R/W	R/W	R/W	
Reset	00		00		0	0	0	0	

PDGIE : Port D collected INT enable

1 : enable

0 : disable

PCGIE : Port C collected INT enable

1 : enable

0 : disable

PBGIE : Port B collected INT enable

1 : enable

0 : disable

PAGIE : Port A collected INT enable

1 : enable

0 : disable

Timers/PWM

The TP292X provides three general purpose Timer/Counters. Timer0 and Timer1 are 10 bit wide, while Timer2 is an 8 bit wide. These timers have individual pre-scaling selection from the separate pre-scalar. These timers/counters are realized as an up-counter with read and write access. The features of these timers are listing as followed.

Features	Timer0	Timer1	Timer2
Width	10 bit	10 bit	8 bit
Period mode	Yes	Yes	Yes
PWM mode	Yes	Yes	No
ICP mode	Yes	Yes	No

There are two types of registers related to the Timer counter. The first is the register that contains the actual value of the Timer counter, which an initial value of the counter can be preloaded. Reading from this register retrieves the contents of the Timer counter. The second type of the associated register is the Timer Control Register that defines the timer options and determines how the timer
is to be used. The device can have the timer clock configured to come from the internal clock source. In addition, the timer clock source can also be configured to come from an external timer pin.

- Period Mode
  - Counter returns to 0 when it matches TM[X]PRD register
  - Set INF flag (TMINTF)
- PWM Mode
  - Counter returns to 0 when it matches TM[X]PRD register
  - When counter value matches TM[X]DUT or TM[X]PRD registers, TMPOE0 register/pin is set/cleared, register and INT flags are set, according to the control registers
- ICP Mode

Timers/PWM Register

[X] = 0 or 1 or 2, it means Time 0, Time 1 and Time 2

	0	1	2
TM[X]CR	0x50(I/O_0x30)	0x4F(I/O_0x2F)	0x66(I/O_##)
TM[X]CNTH	0x3F(I/O_0x1F)	0x4D(I/O_0x2D)	0x65(I/O_##)
TM[X]CNTL	0x52(I/O_0x32)	0x4C(I/O_0x2C)	0x64(I/O_##)
TM[X]PRDH	0x3D(I/O_0x1D)	0x4B(I/O_0x2B)	0x61(I/O_##)
TM[X]PRDL	0x56(I/O_0x36)	0x4A(I/O_0x2A)	0x60(I/O_##)
TM[X]DUTH	0x3E(I/O_0x1E)	0x49(I/O_0x29)	0x63(I/O_##)
TM[X]DUTL	0x5C(I/O_0x3C)	0x48(I/O_0x28)	0x62(I/O_##)

PS. I/O_## no value.

TM[X] CR (Timer[X] Control Register)

Bit	7	6	5	4	3	2	1	0	TM[X]CR
0x00_50	T[X]FOCM	T[X]MODE	T[X]OC[1:0]		Reserved	T[X]PS[2:0]			I/O_0x30
R/W	R/W	R/W	R/W		R	R/W			
Reset	0	0	00		0	000			

T[X]FOCM : Time[X] force compare match at Period Mode
1 : enable
0 : disable

T[X]MODE :Timer[X] Mode
1 : PWM mode
0 : Period mode

T[X] FOCM is auto-cleared after writing `1' .

T[X]OC :Timer[X] output control
00 : pin as IO port
01 ~ 11 : depends on TM[X]MODE, see table below

T[X]PS :Timer[X] clock pre-scalar
000 : no clock
001 : CLK /1
010 : CLK /4
011 : CLK /16
100 : CLK /64
101 : CLK /256
110 : TM[X]I pin falling
111 : TM[X]I pin rising

- TM[X]FOCM
  - Write-only. Any write of 1 to it will generate a forced-match strobe last 1 cycle long. Read from TM[X] FOCM always gets `0' .
  - Affects output waveform only. Counter is not reset, and no INT is generated.
- Mode and waveform output

TM[X]OC[1:0]	TM[X]MODE	
	PWM(1)	Period(0)
00	Pin as IO	Pin as IO
01	Toggle output when TM[X]CNT = PRD	Reserved
10	Output = 1 when TM[X]CNT = 0X00, 0 when TM[X]CNT = DUTY	Clear output when TM[X]CNT = PRD
11	Output = 0 when TM[X]CNT = 0X00, 0 when TM[X]CNT = DUTY	Set output when TM[X]CNT = PRD

TM[X] CNTH (Timer[X] Counter High byte)

Bit	7	6	5	4	3	2	1	0	TM[X]CNTH
0x00_3F	TM[X]CNT[15:8]								I/O_0x1F
R/W	R/W								
Reset	00000000								

TM[X] CNT [15:8]: Timer[X] counter high byte

TM[X] CNTL (Timer[X] Counter Low byte)

Bit	7	6	5	4	3	2	1	0	TM[X]CNTL
0x00_52	TM[X]CNT[7:0]								I/O_0x32
R/W	R/W								
Reset	00000000								

TM[X] CNT [7:0]: Timer[X] counter low byte

TM[X] PRDH (Timer[X] Period High byte)

Bit	7	6	5	4	3	2	1	0	TM[X]PRDH
0x00_3D	TM[X]PRD[15:8]								I/O_0x1D
R/W	R/W								
Reset	00000000								

TM[X] PRD [15:8]: Timer[X] period high byte

TM[X] PRDL (Timer[X] Period Low byte)

Bit	7	6	5	4	3	2	1	0	TM[X]PRDL
0x00_56	TM[X]PRD[7:0]								I/O_0x36
R/W	R/W								
Reset	00000000								

TM[X] PRD [7:0]: Timer[X] period low byte

- TM[X] PRDH/L is not double-buffered. F/W write to TM[X] PRDH/L takes effect immediately.
- In PWM mode
  - If DUTY = 0x00: PWMO is a short pulse of 1 cycle wide.
  - If DUTY = PRD: PWMO is always active.

TM[X] DUTH (Timer[X] Duty High byte)

Bit	7	6	5	4	3	2	1	0	TM[X]DUTH
0x00_3E	TM[X]DUT[15:8]								I/O_0x1E
R/W	R/W								
Reset	00000000								

TM[X] DUT [15:8]: Timer[X] active pulse width high byte

TM[X] DUTL (Timer[X] Duty Low byte)

Bit	7	6	5	4	3	2	1	0	TM[X]DUTL
0x00_5C	TM[X]DUT[7:0]								I/O_0x3C
R/W	R/W								
Reset	00000000								

TM[X] DUT [7:0]: Timer[X] active pulse width low byte

TMICP (Timer Input Capture)

Bit	7	6	5	4	3	2	1	0	TMICP
0x00_2B	T3ICPE	T3ICPP	T2ICPE	T2ICPP	T1ICPE	T2ICPP	T0ICPE	T0ICPP	I/O_0x0B
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	0	

T[x]ICPE : Timer[x] ICP enable

1 : enable

0 : disable ICP, enable Period / PWM mode

T[x]ICPP : Timer[x] ICP trigger polarity

1 : rising edge

0 : falling edge

[x] = 0, 1, 2, 3.

TMINTF (Timer Input Capture)

Bit	7	6	5	4	3	2	1	0	TMINTF
0x00_2C	Reserved		T2PRDIF	Reserved	T1PRDIF	T1DUTIF	T0PRDIF	T0DUTIF	I/O_0x0C
R/W	R		R/W	R	R/W	R/W	R/W	R/W	
Reset	0		0	0	0	0	0	0	

T[x]PRDIF : Timer[x] Period overflow INT flag

1 : flag set

[x] = 0, 1, 2

T[x]DUTIF : Timer[x] MAX overflow or Duty match INT flag

1 : flag set

[x] = 0, 1

- MAX means 0xFFFF
  - TM[x] PRDIF is triggered when TM[x] CNT counts from PRD -> 0.

- TM[x] DUTYIF is triggered when TM[x] CNT counts from MAX -> 0.

- In PWM Mode
  - TM[x] PRDIF is triggered when TM[x] CNT counts from PRD -> 0.
  - TM[x] DUTYIF is triggered when TM[x] CNT matches TM[x] DUT.
- In ICP Mode
  - TM[x] PRDIF is set at the 2nd edge after the trigger edge.
  - TM[x] DUTYIF is set if TM[x] CNT overflow from MAX -> 0.

TMINTE (Timer INT Enable Control)

Bit	7	6	5	4	3	2	1	0	TMINTE
0x00_42	Reserved		T2PRDIE	Reserved	T1PRDIE	T1DUTIE	T0PRDIE	T0DUTIE	I/O_0x22
R/W	R		R/W	R	R/W	R/W	R/W	R/W	
Reset	00		0	0	0	0	0	0	

T[x]PRDIF : Timer[x] Period match INT
1 : enable
0 : disable
[x] = 0, 1, 2

T[x]DUTIF : Timer[x] Duty match or counter overflow INT
1 : enable
0 : disable
[x] = 0, 1

TMPOE0 (Timer 0/1 Pin Output Enable)

Bit	7	6	5	4	3	2	1	0	TMPOE0
0x00_81	TM1PODE	TM1POCE	TM1POBE	TM1POAE	TM0PODE	TM0POCE	TM0POBE	TM0POAE	I/O_##
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	0	

T[x]PODE : TM[x]POD pin on/off
1 : on
0 : off, level according to TM[x]OC[1:0]
T[x]POBE : TM[x]POB pin on/off
1 : on
0 : off, level according to TM[x]OC[1:0]
[x] = 0, 1

T[x]POCE : TM[x]POC pin on/off
1 : on
0 : off, level according to TM[x]OC[1:0]
T[x]POAE : TM[x]POA pin on/off
1 : on
0 : off, level according to TM[x]OC[1:0]

Analog Comparator

The analog comparator compares the input values on the positive pin ACMxP and the negative pine ACMxN. When the voltage on the positive pin is higher than the voltage on the negative pin, the Analog Comparator Output is set to one. There are 3 sets of analog comparators and the comparators' output can be triggered a separate interrupt.

Two sets of registers are associated with analog comparator's module; Analog Comparator Control, and Status Register.

Analog Comparator Register

ACMCR (ACMP Control)

Bit	7	6	5	4	3	2	1	0	ACMCR
0x00_28	Reserved	ACMCE	ACMBE	ACMAE	Reserved	ACMCO	ACMBO	ACMAO	I/O_0x08
R/W	R	R/W	R/W	R/W	R	R	R	R	
Reset	0	0	0	0	0	0	0	0	

ACM[x]E : ACMP [x] analog enable
1 : enable
0 : disable

ACM[x]O : ACMP [x] output
1 : P > N
0 : P < N

[x] = A, B, C

ACMICR (ACMP INT Control)

Bit	7	6	5	4	3	2	1	0	ACMICR
0x00_3C	Reserved	ACMDIF	ACMIE	ACMIF	Reserved	ACMCIM	ACMBIM	ACMAIM	I/O_0x1C
R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	0	

ACMDIF : ACMP D INT flag
1 : flag set

ACMIE : ACMP A/B/C INT on/off
1 : enable
0 : disable

ACMIF : ACMP A/B/C INT flag
1 : flag set

ACM[x]IM : ACMP [x] INT mask
1 : enable
0 : disable

[x] = A, B, C.

- ACMP A/B/C share 1 INT vector and 1 INT enable bit.
- ACMIF is set when either of ACM(A/B/C) output transits.
- When ACM(A/B/C)IM = 1, corresponding ACMP can trigger ACMIF.
- ACMIF and ACMDIF are automatically cleared by H/W upon INT processing.

Analog to Digital Converter

The device features 10 bit single-ended Analog to Digital Converter (ADC). It converts analog input channels into a 10-bit value with maximum conversion rate 200KSPS. The ADC is enabled by setting the ADC enable bit “ADCE” and is started the conversion process by writing a logical one to the ADC Start Conversion bit, “ADCSC”. This ADCSC bit stays high as long as the conversion is in progress and will be set to zero by hardware when the conversion is completed.

The ADC data register ADCH (ADC result High byte) and ADCL (ADC result Low byte) stores the 10 bit result. By default, the result is presented right adjusted, but can optionally be set left adjusted by setting the bit “ADCLAR”. To prevent reading mis-matched ADCH/L, an ADCL read action will block ADC from updating ADCH/L. ADCH read action resumes ADC updating to ADCH/L. Thus, if both ADCH/L is needed, ADCL must be read first.

Analog to Digital Converter Register

ADCMUX (ADC VREF and Input Selection)

Bit	7	6	5	4	3	2	1	0	ACMICR
0x00_27	ADCVS[1:0]		Reserved		ADCIS[3:0]				I/O_0x07
R/W	R/W		R		R/W				
Reset	00		00		0000				

ADCVS : VREF selection

- 00 : VDD
- 01 : reserved
- 10 : internal VREF
- 11 : reserved

ADCIS[3:0] : ADC input selection

- 0000 ~ 0111 : ADCI0 ~ 7 pin
- 1000 : VSS
- 1001 : internal VREF
- 1010 : AREF pin
- 1011 ~ 1111 : reserved

- F/W write to ADCMUX is not double-buffered, so it will take immediately. Changing ADCMUX in the middle if conversion may ruin the current result.

ADCCRA (ADC Control A)

Bit	7	6	5	4	3	2	1	0	ADCCRA
0x00_26	ADCE	ADCSC	ADCATE	ADCIF	ADCIE	ADCPS[2:0]			I/O_0x06
R/W	R/W	R/W	R/W	R/W	R/W	R/W			
Reset	0	0	0	0	0	000			

ADCE : ADC analog on/off

- 1 : enable
- 0 : disable

ADCATE : ADC auto-conversion

- 1 : enable
- 0 : disable

ADCIE : ADC INT on/off

- 1 : enable
- 0 : disable

ADCSC : Start conversion

- 1 : start and on-going
- 0 : finished

ADCIF : ADC INT flag

- 1 : conversion complete

ADCPS : ADC clock dividing factor

- 001 : 2
- 010 : 4
- 011 : 8
- 100 : 16
- 101 : 32
- 110 : 64
- 111 : 128

- When ADCE = 0, all ADC analog circuit is hut down and consumes no power.
- ADCSC keeps at `1' while conversion is on-going. H/W automatically clear ADCSC upon conversion completion.

ADCCRB (ADC Control B)

Bit	7	6	5	4	3	2	1	0	ACMICR
0x00_23	Reserved			ADCLAR	Reserved	ADCTS[2:0]			I/O_0x03
R/W	R			R/W	R	R/W			
Reset	000			0	0	000			

ADCLAR : ADC data alignment

1 : left adjust

0 : right

ADCTS : ADC auto-trigger

000 : self-trigger (continuous free run)

001 : ACMP A

010 : reserved

011 : Timer0 PRD overflow

100 : Timer1 PRD overflow

101 : Timer2 PRD overflow

110 : reserved

111 : reserved

- ADCLAR = 1, ADCH/L = { data[9:0], 6'b000000}
- ADCLAR = 0, ADCH/L = { 6'B000000, data[9:0] }

ADCH (ADC result High byte)

Bit	7	6	5	4	3	2	1	0	TM[X]DUTH
0x00_25	ADC[15:8]								I/O_0x05
R/W	R								
Reset	00000000								

ADC [15:8]: ADC RESULT high byte

ADCL (ADC result Low byte)

Bit	7	6	5	4	3	2	1	0	TM[X]DUTH
0x00_24	ADC[7:0]								I/O_0x04
R/W	R								
Reset	00000000								

ADC [7:0]: ADC RESULT high byte

- To prevent reading mis-matched ADCH/L, an ADCL read action will block ADC from updating ADCH/L. Thus, if both ADCH/L is needed, ADCL must be read first.
- If ADC data is left-adjusted (ADCLAR = 1) and only 8 bit result is needed, it is OK to read ADCH only.

SFR register List

DS#	IO#	Name	B7	B6	B5	B4	B3	B2	B1	B0
0x00_20	0x00	PWRR0	CKDPRTD	CKDPRTC	CKDPRTB	CKDPRTA	CKDTM3	CKDTM2	CKDTM1	CKDTM0
0x00_21	0x01	PWRR1	=	=	CKDPRTEF	CKDUSI	=	=	CKDADC	CKDACMP
0x00_23	0x03	ADCCRB	=	=	=	ADCLAR	=	ADCTS[2:0]		
0x00_24	0x04	ADCL	ADC[7:0]							
0x00_25	0x05	ADCH	ADC[15:8]							
0x00_26	0x06	ADCCRA	ADCE	ADCSC	ADCATE	ADCIF	ADCIE	ADCPS[2:0]		
0x00_27	0x07	ADCMUX	ADCVS[1:0]		=	=	ADCIS[3:0]			
0x00_28	0x08	ACMCR	=	ACMCE	ACMBE	ACMAE	=	ACMCO	ACMBO	ACMAO
0x00_2B	0x0B	TMICP	=	=	=	=	T1ICPE	T1ICPP	T0ICPE	T0ICPP
0x00_2C	0x0C	TMINTF	=	=	T2PRDIF	=	T1PRDIF	T1DUTIF	T0PRDIF	T0DUTIF
0x00_32	0x12	PAIM	PAIM[7:0]							
0x00_33	0x13	GIO0	=							
0x00_34	0x14	GIO1	=							
0x00_35	0x15	GIO2	=							
0x00_36	0x16	PBDI	PBDI[7:0]							
0x00_37	0x17	PBDR	PBDR[7:0]							
0x00_38	0x18	PBDO	PBDO[7:0]							
0x00_39	0x19	PADI	PADI[7:0]							
0x00_3A	0x1A	PADR	PADR[7:0]							
0x00_3B	0x1B	PADO	PADO[7:0]							
0x00_3C	0x1C	ACMICR	=	ACMDIF	ACMIE	ACMIF	=	ACMCIM	ACMBIM	ACMAIM
0x00_3D	0x1D	TM0PRDH	TM0PRD[9:8]							
0x00_3E	0x1E	TM0DUTH	TM0DUT[9:8]							
0x00_3F	0x1F	TM0CNTH	TM0CNT[9:8]							
0x00_40	0x20	PBIM	PBIM[7:0]							
0x00_41	0x21	WDTCSR	WDIF	WDIE	WDCE	WDE	WDP[3:0]			
0x00_42	0x22	TMINTE	=	=	T2PRDIE	=	T1PRDIE	T1DUTIE	T0PRDIE	T0DUTIE
0x00_43	0x23	TMPSC	TMPSH	=	=	=	=	=	=	TMPSR
0x00_46	0x26	CLKPR	CLKPCE	=	=	=	CLKPS[3:0]			
0x00_48	0x28	TM1DUTL	TM1DUTY[7:0]							
0x00_49	0x29	TM1DUTH	TM1DUTY[9:8]							
0x00_4A	0x2A	TM1PRDL	TM1PRD[7:0]							
0x00_4B	0x2B	TM1PRDH	TM1PRD[9:80]							
0x00_4C	0x2C	TM1CNTL	TM1CNT[7:0]							
0x00_4D	0x2D	TM1CNTH	TM1CNT[9:8]							
0x00_4F	0x2F	TM1CR	T1FOCM	T1MODE	T1OC[1:0]		=	T1PS[2:0]		
0x00_50	0x30	TM0CR	T0FOCM	T0MODE	T0OC[1:0]		=	T0PS[2:0]		
0x00_52	0x32	TM0CNTL	TM0CNT[7:0]							
0x00_54	0x34	MSR	=	=	=	=	WDRF	LVRF	PINRF	PORF
0x00_55	0x35	MCR	LVRSLP	PORTUD	SLPE	SLPM[1:0]		LVRSLPE	=	=
0x00_56	0x36	TM0PRDL	TM0PRD[7:0]							
0x00_5A	0x3A	PORTIF	=	=			PDGIF	PCGIF	PBGIF	PAGIF
0x00_5B	0x3B	PORTIE	=	=			PDGIE	PCGIE	PBGIE	PAGIE
0x00_5C	0x3C	TM0DUTL	TM0DUTY[7:0]							
0x00_5D	0x3D	SPL	SP[7:0]							
0x00_5E	0x3E	SPH	SP[15:8]							
0x00_5F	0x3F	SR	I	T	H	S	V	N	Z	C
0x00_64	=	TM2CNTL	TM2CNT[7:0]							
0x00_66	=	TM2CR	T2FOCM	T2MODE	T2OC[1:0]		=	T2PS[2:0]		
0x00_70	=	PCDO	PCDO[3:0]							
0x00_71	=	PCDI	PCDI[3:0]							
0x00_72	=	PCDR	PCDR[3:0]							
0x00_73	=	PCIM	PCIM[3:0]							
0x00_74	=	PDDO	PDDO[3:0]							
0x00_75	=	PDDI	PDDI[3:0]							
0x00_76	=	PDDR	PDDR[3:0]							
0x00_77	=	PDIM	PDIM[3:0]							
0x00_81	=	TMPOE0	T1PODE	T1POCE	T1POBE	T1POAE	T0PODE	T0POCE	T0POBE	T0POAE

Instruction List

Mnemonics	Description	Mnemonics	Description
ADD	Add without Carry	BRNE	Branch if Not Equal
ADC	Add with Carry	BRCS	Branch if Carry Set
ADIW	Add immediate to Word	BRCC	Branch if Carry Cleared
SUB	Subtract without Carry	BRSH	Branch if Same or Higher
SUBI	Subtract Immediate	BRLO	Branch if Lower
SBC	Subtract with Carry	BRMI	Branch if Minus
SBCI	Subtract Immediate with Carry	BRPL	Branch if Plus
SBIW	Subtract Immediate from Word	BRGE	Branch if Greater or Equal, Signed
AND	Logical AND	BRLT	Branch if Less Than, Signed
ANDI	Logical AND with Immediate	BRHS	Branch if Half Carry Flag Set
OR	Logical OR	BRHC	Branch if Half Carry Flag Cleared
ORI	Logical ORI	BRTS	Branch if T Flag Set
EOR	Exclusive OR	BRTC	Branch if T Flag Cleared
COM	One's Complement	BRVS	Branch if Overflow Flag is Set
NEG	Two's Complement	BRVC	Branch if Overflow Flag is Cleared
SBR	Set Bit(s) in Register	BRIE	Branch if Interrupt Enable
CBR	Clear Bit(s) in Register	BRID	Branch if Interrupt Disable
INC	Increment	MOV	Copy Register
DEC	Decrement	LDI	Load Immediate
TST	Test for Zero or Minus	LDS	Load Direct from data space
CLR	Clear Register	LD	Load Indirect and Post-Increment
SER	Set Register	LDD	Load Indirect with Displacement
RJMP	Relative Jump	STS	Store Direct to Data Space
IJMP	Indirect Jump to (Z)	ST	Store Indirect and Post-Increment
JMP	Jump	STD	Store Indirect with Displacement
RCALL	Relative Call Subroutine	LPM	Load Program Memory
ICALL	Indirect Call to (Z)	IN	In From I/O Location
CALL	Call Subroutine	OUT	Out To I/O Location
RET	Subroutine Return	PUSH	Push Register on Stack
RETI	Interrupt Return	POP	Pop Register from Stack
CPSE	Compare, Skip if Equal	WDR	Watchdog Reset
CP	Compare	SEH	Set Half Carry Flag in SR
CPC	Compare with Carry	CLH	Clear Half Carry Flag in SR
CPI	Compare with Immediate	BREAK	Break
SBRC	Skip if Bit in Register Cleared	LSL	Logical Shift Left
SBRS	Skip if Bit in Register Set	LSR	Logical Shift Register

SBIC	Skip if Bit in I/O Register Cleared	ROL	Rotate Left Through Carry
SBIS	Skip if Bit in I/O Register set	ROR	Rotate Right Through Carry
BRBS	Branch if Status Flag Set	ASR	Arithmetic Shift Right
BRBC	Branch if Status Flag Cleared	SWAP	Swap Nibbles
BREQ	Branch if Equal	BEST	Flag Set
BCLR	Flag Clear	CLN	Clear Negative Flag
SBI	Set Bit in I/O Register	SEZ	Set Zero Flag
CBI	Clear Bit in I/O Register	CLZ	Clear Zero Flag
BST	Bit Store from to T	SEI	Global Interrupt Enable
BLD	Bit load from T to Register	CLI	Global Interrupt Disable
SEC	Set Carry	SES	Set Signed Test Flag
CLC	Clear Carry	CLS	Clear Signed Test Flag
SEN	Set Negative Flag	SEV	Set Two's Complement Overflow
CLV	Clear Two's Complement Overflow	NOP	No Operation
SET	Set T in SR	SLEEP	Sleep
CLT	Set T in SR		

Fuse Option List

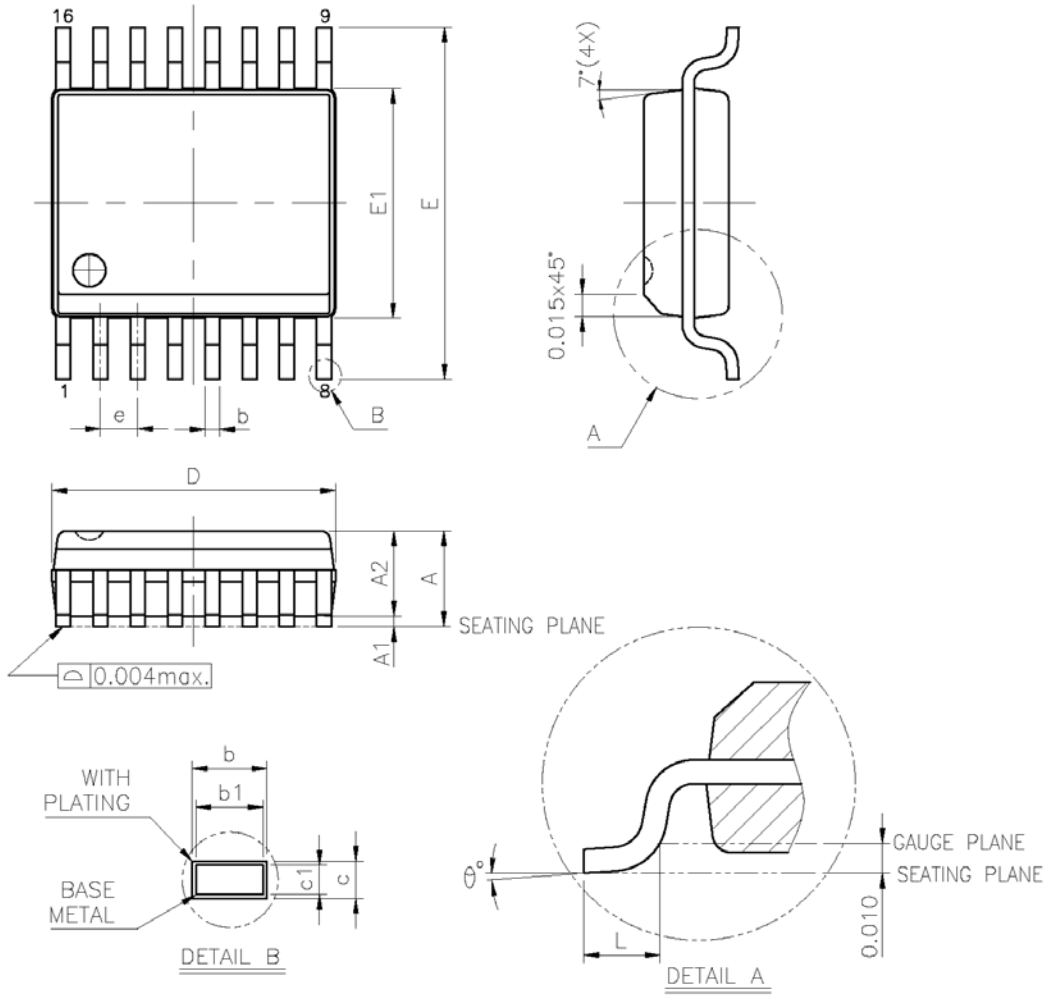
Purpose	Description
OTP page	1KW program at OTP page 0 Fuse option page 0
	1KW program at OTP page 1 Fuse option page 0
	2KW of program at OTP page 0 + page 1 Fuse option page 0
	Reserved
OTP read protection	If programmed, OTP F/W code can not be read by OTP writer
Enable CPU clock output to pin	Disable pre-scaled system clock to output to IO pin
	Enable
LVR enable and level	LVR disabled
	1.8V
	2.7V
	4.3V
	Reserved
WDT enable/disable	WDT off upon reset
	WDT on upon reset
Oscillator type	Pin
	Calibrated RC, 8M
	WDT oscillator, 128KHz
	Fast XTAL, 4～16MHz
	Reserved (32KHz XTAL)
	Reserved
Warmup time selection	Power start-up delay selection; control both RESET and SLEEP warm-up delay; 4 choices: longest, long, short, shortest
Timer 0 PWM output pin enable/disable	TM0 PWM output pin selection 1: not PWM output 0: PWM output [3:0]: TM0POC～A
Timer 1 PWM output pin enable/disable	TM1 PWM output pin selection 1: not PWM output 0: PWM output [3:0]: TM1POC～A
ACMP pin enable/disable	ACMP input pin selection 1: ACMP input disable 0: ACMP input enable [5:0]: ACMP CP/DN/.../AP/AN
ADC input pin enable/disable	ADC input pin selection 1: ADC input disable 0: ADC input enable [3:0]: ADCI3～0
ADC external VREF pin enable/disable	ADC AREF pin disable
	ADC AREF pin enable, when internal or external VREF is selected for ADC

DC Electrical Characteristics

Group	Item	Symbol	Min	Typ	Max	Unit	VDD	Note
chip voltage	Normal mode		**3**	**=**	**5.5**	V	=	CPU 10MHz
Chip current	Normal mode			**5.3**		mA	5V/ 3.3V	RC 8MHz CPU 8MHz IO quiet
				0.36		mA		RC 8MHz CPU 8MHz/256 IO quiet
	Idle mode			**1.2**		mA		RC 8MHz CPU 8MHz Only CPU off
				0.6		mA		RC 8MHz CPU 8MHz All CLK off
	Power-down mode			**45**		uA	5V	
				35		uA	3.3V	
IO	Port output high current	**IoL**		**17**		mA	5V	VoL = 2.5v
	Port output high current	**IoH**		**5**		mA		VoH = 2.5v
	Port and RESETn pin weak pull-up R			**400**		Kohm		
	Port output high current	**IoL**		**9.6**		mA	3.3V	VoL = 1.65v
	Port output high current	**IoH**		**3.3**		mA		VoH = 1.65v
	Port weak pull-up R			**400**		Kohm		RESETn pin the same
POR	Reset active VDD level		**=**	**=**	**0.8**	V	=	
	VDD rising slew rate		**=**	**=**	**10**	mS		
LVR	Reset active VDD level			**1.8**		V	=	Low level
				2.7		V		Medium level
				4.5		V		High level
	Hysteresis			**0.1**		V		
ACMP	Common voltage		**0.5**	**=**	**4.5**	V	5V	
			0.3	**=**	**3**	V	3.3V	
	Differential voltage		**=**	**=**	**20**	mV	5V/ 3.3V	
	Response time		**=**	**=**	**10**	uS		
ADC	Internal VREF level			**1.2**		V	5V/ 3.3V	
	Input range		**0.1**	**=**	**Note**	V		
	Conversion rate		**=**	**=**	**100**	KHz		

Package Information

SSOP 16

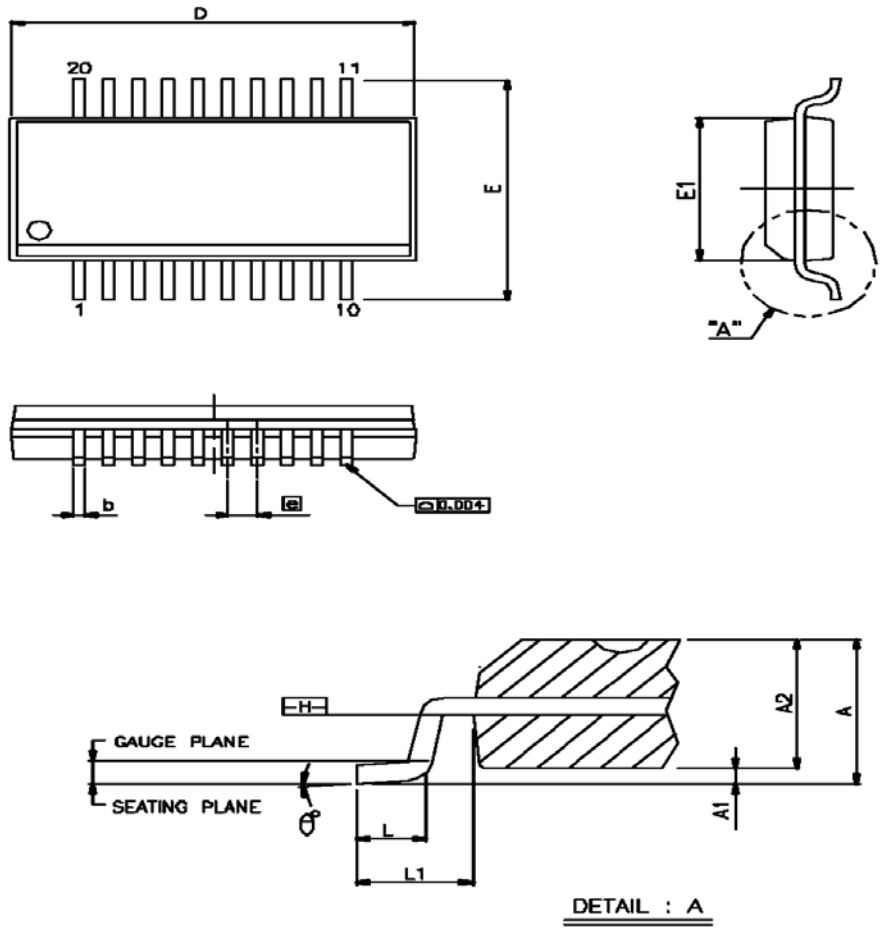


SYMBOLS	MIN.	NOM.	MAX.
A	0.053	—	0.069
A1	0.004	—	0.010
A2	0.049	—	0.059
b	0.008	—	0.012
b1	0.008	0.010	0.011
c	0.007	—	0.010
c1	0.007	0.008	0.009
D	0.189	0.193	0.197
E1	0.150	0.154	0.157
E	0.228	0.236	0.244
L	0.016	—	0.050
e	0.025 BASIC		
θ°	0	—	8

UNIT : INCH

NOTES:
1. JEDEC OUTLINE : MO-137 AB
2. DIMENSIONS "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .15mm (.006in) PER SIDE.
3. DIMENSIONS "E1" DOES NOT INCLUDE INTER-LEAD FLASH, OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .25mm (.010in) PER SIDE.

SSOP 20



SYMBOLS	MIN.	NOM.	MAX.
A	0.053	0.064	0.069
A1	0.004	0.006	0.010
A2	–	–	0.059
b	0.008	–	0.012
C	0.007	–	0.010
D	0.337	0.341	0.344
E	0.228	0.236	0.244
E1	0.150	0.154	0.157
e	0.025 BASIC		
L	0.016	0.025	0.050
L1	0.041 BASIC		
θ°	0°	–	8°

UNIT : INCH

NOTES:

1. JEDEC OUTLINE : MO-137 AD
2. DIMENSION D DOES NOT INCLUDE MOLD PROTRUSIONS OR GATE BURRS. MOLD PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.006" PER SIDE. DIMENSION E1 DOES NOT INCLUDE INTERLEAD MOLD PROTRUSIONS. INTERLEAD MOLD PROTRUSIONS SHALL NOT EXCEED 0.010" PER SIDE.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.004" TOTAL IN EXCESS OF b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR INTRUSION SHALL NOT REDUCE DIMENSION b BY MORE THAN 0.002" AT LEAST.