## General Description

The TP2804/TP2804T is an 8-bit microcontroller which has an in-system programmable FLASH EPROM for firmware updated. Its instruction set is fully compatible with the standard 8051. It contains a 64K-byte FLASH EPROM, 512-byte on-chip RAM, four 8-bit bi-directional and bit-addressable I/O ports, an additional 4-bit I/O port, three 16-bit timer/counters and one serial port.

## Applications

- LCD Monitor/TV
- CAT TV
- DVR
- Security

## Features

- Fully static design of 8-bit CMOS microcontroller
- Running clock up to 40MHz
- 64K-byte FLASH EPROM
- Low standby current at full supply voltage
- 512-byte on-chip RAM (including 256-byte AUX-RAM, software selectable)
- 64K-byte program memory address space and 64K-byte data memory address space
- Four 8-bit bi-directional ports
- One 4-bit multipurpose programmable port
- Three 16-bit timer/counters
- One full duplex serial port
- Eight-source and two-level interrupt capability
- Built-in power management
- Code protection
- Internal power-on-reset (TP2804T/5V only)
- Two voltage types: 3.3V and 5V
- Package Forms: DIP40, PLCC44 and PQFP44

## Ordering Information

TP2804 □ □ □

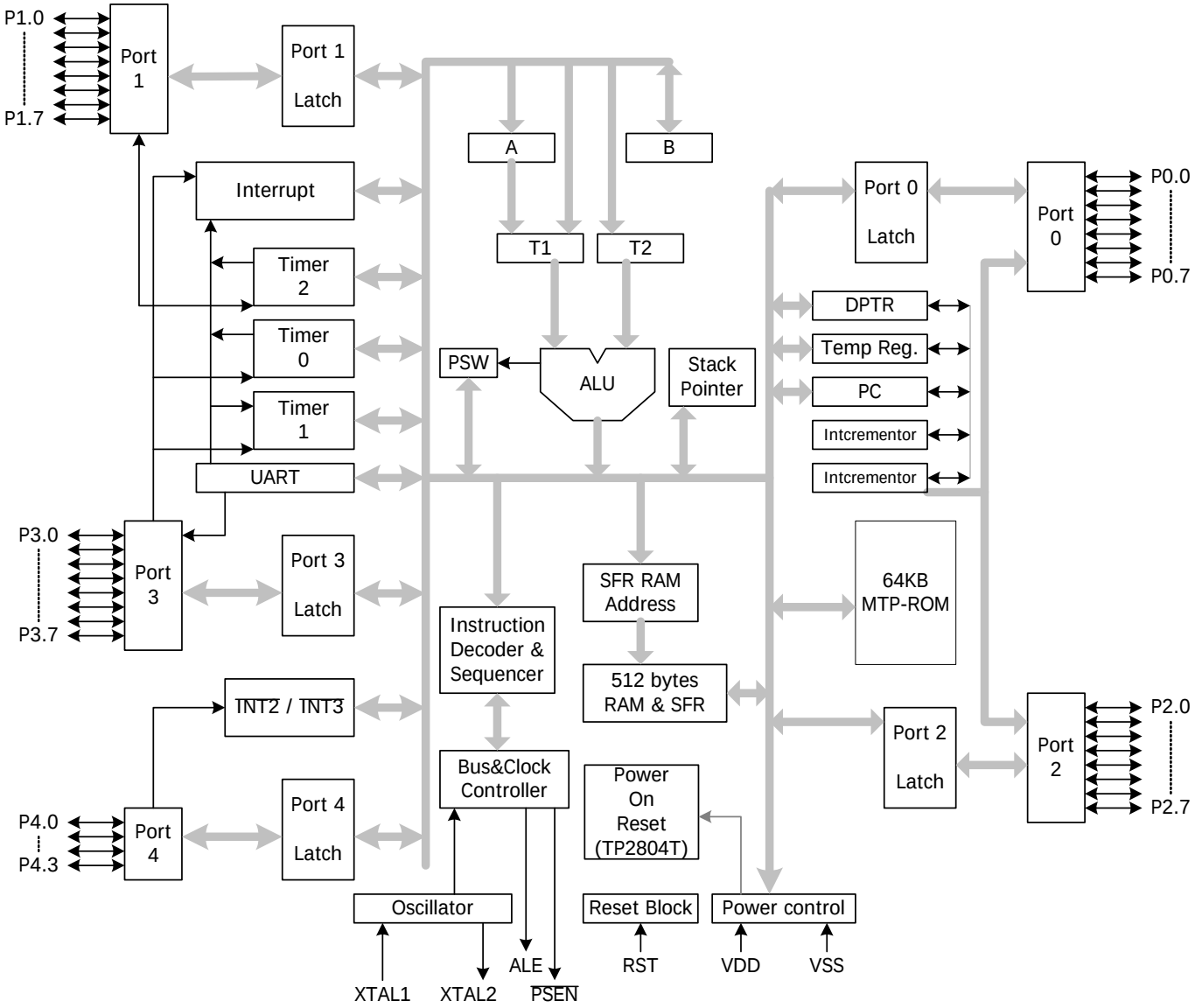
- Package Type 2
- Package Type 1
- Voltage

TP2804T H □ □

- Package Type 2
- Package Type 1
- 5V only

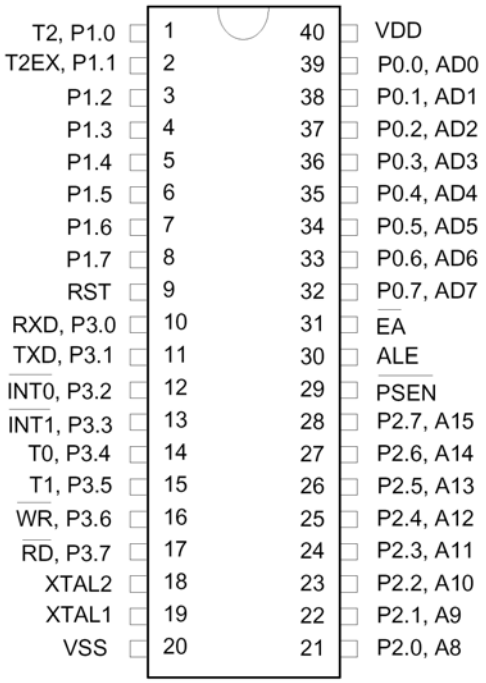
| | |
|---|---|
| **Voltage** | L: 3.3V<br>H: 5V |
| **Package Type 1** | P: DIP<br>C: PLCC<br>Q: PQFP |
| **Package Type 2** | G:Green<br>N:Pb free |

## Block Diagram

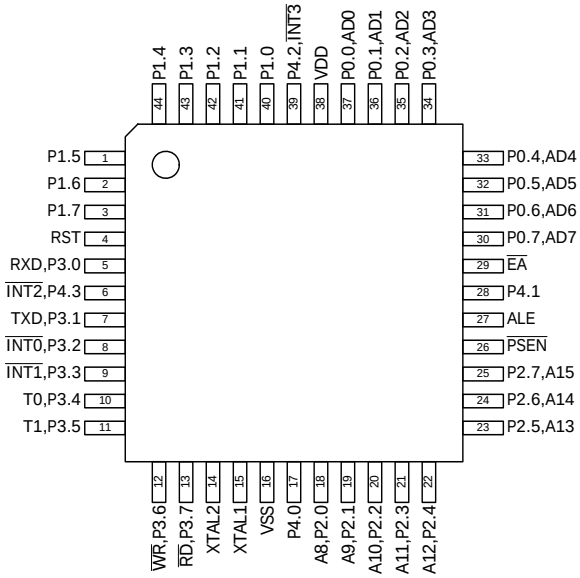


## Pin Configuration

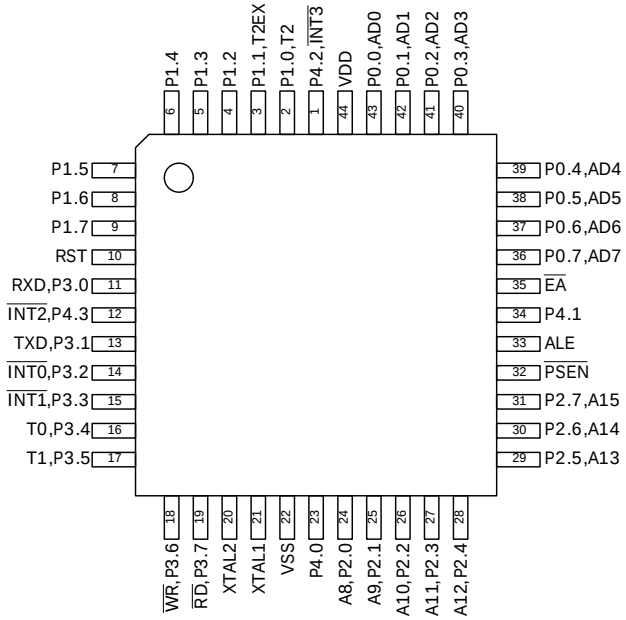
### 40-PIN DIP




### 44-PIN PQFP




### 44-PIN PLCC



## Pin Description

| Symbol | Type | Description |
|---|---|---|
| $\overline{EA}$ | I | EXTERIAL ACCESS ENABLE: This pin should be forced to high level and the program counter is within the 64 KB area. |
| $\overline{PSEN}$ | O/H | PROGRAM STORE ENABLE: When internal ROM access is performed, no $\overline{PSEN}$ strobe signal output is originated from this pin. |
| ALE | O/H | ADDRESS LATCH ENABLE: ALE is used to enable the address latch that separates the address from the data on Port 0. ALE runs at 1/6$^{th}$ of the oscillator frequency. An ALE pulse is omitted during external data memory accesses. |
| RST | I/L | RESET: A high on this pin for two machine cycles resets the device while the oscillator is running. |
| XTAL1 | I | CRYSTAL 1: This is the crystal oscillator input. The pin may be driven by an external clock. |
| XTAL2 | O | CRYSTAL 2: This is the crystal oscillator output. It is the inversion of XTAL1. |
| $V_{SS}$ | I | GROUND: Ground potential. |
| $V_{DD}$ | I | POWER SUPPLY: Supply voltage for operation.<br>TP2804T operates in 5V only. |
| P0.0 - P0.7 | I/O/D | PORT 0: Function is the same as that of standard 8051. |
| P1.0 - P1.7 | I/O/H | PORT 1: Function is the same as that of standard 8051. |
| P2.0 - P2.7 | I/O/H | PORT 2: Function is the same as that of standard 8051. |
| P3.0 - P3.7 | I/O/H | PORT 3: Function is the same as that of standard 8051. |
| P4.0 - P4.3 | I/O/H | PORT 4: A bi-directional I/O port with internal pull-ups. |

NOTES: TYPE I: input; O: output; I/O: bi-directional; H: pull-high; L: pull-low; D: open drain at output, except power up.

## Functional Description

The TP2804/TP2804T architecture consists of a core controller surrounded by various registers, four general-purpose I/O port, 512-byte RAM, three timer/counters, a serial port. Its processor supports 111 different opcodes and references, both 64K program address space and 64K data storage space.

### RAM

The internal data RAM of TP2804/TP2804T has 512 bytes and is divided into two banks: scratchpad 256-byte RAM and 256-byte AUX-RAM. These RAMs are addressed by different ways:

- RAM 00H-7FH can be addressed directly and indirectly as the same as in 8051. Address pointers are R0 and R1 of the selected register bank.
- RAM 80H-FFH can only be addressed indirectly as the same as in 8051. Address pointers are R0 and R1 of the selected registers bank.
- AUX-RAM 00H-FFH is addressed indirectly as the same way to access external data memory with the MOVX instruction. Address pointers are R0 and R1 of the selected register bank and DPTR register. The AUX-RAM is disabled after a reset. Setting the bit 4 in CHPCON register will enable the access to on-chip AUX-RAM.

### Timers 0, 1, and 2

Timers 0, 1, and 2 each consist of two 8-bit data registers. These are called TL0 and TH0 for Timer 0, TL1 and TH1 for Timer 1, and TL2 and TH2 for Timer 2. The TCON and TMOD registers provide control functions for timers 0 and 1. The T2CON register provides control functions for Timer 2. RCAP2H and RCAP2L are used as auto-reload or capture registers for Timer 2 as it in 8051.

The operations of Timer 0 and Timer 1 are the same as the standard 8051. Timer 2 is a 16-bit timer/counter that is configured and controlled by the T2CON register. Like timers 0 and 1, Timer 2 can operate as either an external event counter or as an internal timer, depending on the setting of bit C/T2 in T2CON. Timer 2 has three operating modes: capture, auto-reload, and baud rate generator. The clock speed at capture or auto-reload mode is the

same as that of timers 0 and 1.

### $\overline{INT2}$ / $\overline{INT3}$

Two additional external interrupts, $\overline{INT2}$ and $\overline{INT3}$, whose functions are similar to those of external interrupt 0 and 1 in the XICON (External Interrupt Control) register. The XICON register is bit-addressable but is not a standard register in the standard 8051. Its address is at 0C0H. To set/clear bits in the XICON register, one can use the "SETB ($\overline{INT3}$) bit" instruction.

### XICON – external interrupt control (C0H)

| PX3 | EX3 | IE3 | IT3 | PX2 | EX2 | IE2 | IT2 |
|---|---|---|---|---|---|---|---|

PX3: External interrupt 3 priority high if set.

EX3: External interrupt 3 enable if set.

IE3: If IT3 = 1, IE3 is set/cleared automatically by hardware when interrupt is detected/serviced.

IT3: External interrupt 3 is falling-edge/low-level triggered when this bit is set/cleared by software.

PX2: External interrupt 2 priority high if set.

EX2: External interrupt 2 enable if set.

IE2: If IT2 = 1, IE2 is set/cleared automatically by hardware when interrupt is detected/serviced.

IT2: External interrupt 2 is falling-edge/low-level triggered when this bit is set/cleared by software.

### Eight-source Interrupt Information

| Interrupt Source | Vector Address | Polling Sequence Within Priority Level | Enable Required Settings | Interrupt Type Edge/Level |
|---|---|---|---|---|
| External Interrupt 0 | 03H | 0 (highest) | IE.0 | TCON.0 |
| Timer/Counter 0 | 0BH | 1 | IE.1 | - |
| External Interrupt 1 | 13H | 2 | IE.2 | TCON.2 |
| Timer/Counter 1 | 1BH | 3 | IE.3 | - |
| Serial Port | 23H | 4 | IE.4 | - |
| Timer/Counter 2 | 2BH | 5 | IE.5 | - |
| External Interrupt 2 | 33H | 6 | XICON.2 | XICON.0 |
| External Interrupt 3 | 3BH | 7 (lowest) | XICON.6 | XICON.3 |

### Watchdog Timer

The Watchdog timer is a free-running timer that can be programmed by the user to serve as a system monitor, a time-base generator or an event timer. It is basically a set of divider that divides the system clock and the divider output is selectable and determines the time-out interval for the time-out system monitor. This is important in the real-time control applications. In case of power glitches or electro-magnetic interference, the processor may begin to execute errant code. If this is left unchecked, the entire system may crash. The watchdog time-out selection will result in different time-out values depending on the clock speed, and the watchdog timer will be disabled on reset. In general, software should restart the watchdog timer to put it into a known state. The control bits that support the watchdog timer are discussed as follows:

**Watchdog Timer Control Register (8FH)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | ENW | CLRW | WIDL | - | - | PS2 | PS1 | PS0 |

NOTES:

- ENW: Enable watchdog if set.
- CLRW: Clear watchdog timer and prescaler if set. This flag will be cleared automatically.
- WIDL: If this bit is set, the watchdog is enabled under IDLE mode. If cleared, the watchdog is disabled under IDLE mode. Default is cleared.
- PS2, PS1, PS0: Watchdog prescaler timer select. Prescaler is selected when set PS2~0 as follows:

| PS2 | PS1 | PS0 | Prescaler Select |
|---|---|---|---|
| 0 | 0 | 0 | 2 |
| 0 | 1 | 0 | 4 |
| 0 | 0 | 1 | 8 |
| 0 | 1 | 1 | 16 |
| 1 | 0 | 0 | 32 |
| 1 | 0 | 1 | 64 |
| 1 | 1 | 0 | 128 |
| 1 | 1 | 1 | 256 |

### Clock

The TP2804/TP2804T should be used with either a crystal oscillator or an external clock. Internally, the clock is divided by twelve before it is used by default. This makes the TP2804/TP2804T relatively insensitive to duty cycle variations in the clock.

### Crystal Oscillator

The TP2804/TP2804T incorporates a built-in crystal oscillator. To make the oscillator work, a crystal must be connected across pins XTAL1 and XTAL2. In addition, a load capacitor must be connected from each pin to ground, and a resistor must also be connected from XTAL1 to XTAL2 to provide a DC bias when the crystal frequency is above 24 $MH_Z$.

### External Clock

An external clock should be connected to pin XTAL1. Pin XTAL2 should be left unconnected. The XTAL1 input is a CMOS-type input as required by the crystal oscillator. Consequently, the external clock signal should have an input of one level greater than 3.5 volts.

## Power Management

### Idle Mode

By setting the IDL bit in the PCON register, the idle mode is set up. In the idle mode, the internal clock to the processor is stopped. The peripherals and the interrupt logic continue to be clocked. The processor will exit idle mode when either an interrupt or a reset occurs.

### Power-down Mode

When the PD bit in the PCON register is set, the processor enters the power-down mode. In this mode, all of the clocks are stopped including the oscillator. To exit from the power-down mode, it is by a hardware reset or external interrupts $\overline{INT0}$ to $\overline{INT3}$ when enabled and set to edge triggered.

### Reset

The external RESET signal is sampled at S5P2. To take effect, it must be held high for at least two machine cycles while the oscillator is running. An internal trigger circuit in the reset line is used to deglitch the reset line when the TP2804 is used with an external RC network. The reset logic also has a special glitch removal circuit that ignores glitches on the reset line. During reset, the ports are initialized to FFH, the stack pointer to 07H, PCON (with the exception of bit 4) to 00H, and all of the other SFR registers except SBUF to 00H. SBUF is not reset.

TP2804T equips an internal power-on-reset logic whenever the VDD supply voltage declines below a preset threshold, keeping it asserted for at least 240ms after VDD has risen above the reset threshold. And the external reset circuit can be removed.

TP2804/TP2804T Special Function Registers (SFRs) and Reset Values

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| F8 | | | | | | | | | FF |
| F0 | +B<br>00000000 | | | | | | | | F7 |
| E8 | **ISP_CTRL<br>00000000** | **ISP_ADDR<br>00000000** | | | | | | | EF |
| E0 | +ACC<br>00000000 | | | | | | | | E7 |
| D8 | +P4<br>xxxx1111 | | | | | | | | DF |
| D0 | +PSW<br>00000000 | | | | | | | | D7 |
| C8 | +T2CON<br>00000000 | | RCAP2L<br>00000000 | RCAP2H<br>00000000 | TL2<br>00000000 | TH2<br>00000000 | | | CF |
| C0 | XICON<br>00000000 | | | | | | | | C7 |
| B8 | +IP<br>00000000 | | | | | | | **CHPCON<br>0xx00000** | BF |
| B0 | +P3<br>00000000 | | | | | | | | B7 |
| A8 | +IE<br>00000000 | | | | | | | | AF |
| A0 | +P2<br>11111111 | | | | | | | | A7 |
| 98 | +SCON<br>00000000 | SBUF<br>xxxxxxxx | | | | | | | 9F |
| 90 | +P1<br>11111111 | | | | | | | | 97 |
| 88 | +TCON<br>00000000 | TMOD<br>00000000 | TL0<br>00000000 | TL1<br>00000000 | TH0<br>00000000 | TH1<br>00000000 | | **WDTC<br>00000000** | 8F |
| 80 | +P0<br>11111111 | SP<br>00000111 | DPL<br>00000000 | DPH<br>00000000 | | | | PCON<br>00110000 | 87 |

## In-System Programming Control Register (CHPCON)

The TP2804/TP2804T equips one main Flash EPROM bank of 64K bytes for application program, but it can be set for a maximum of 4K-byte loader program and 60K-byte application program. **The size of application program depends on the content (bit5~bit7) of address FFFFh in the 64K bytes. If one unit is 512 bytes, user can set for eight different units (000~111). For example, if the data of address FFFFh is 000XXXXXb, the application program range is from address 0000h to EFFFh and loader program range is from address F000h to FFFFh. If the data of address FFFFh is 001XXXXXb, the application program range is from address 0000h to F1FFh and loader program range is from address F200h to FFFFh and so on.** User can enter ISP mode with two different ways. One is by software, for example, using "JMP F000h" to loader program address. The other is by hardware. In the normal operation, the microcontroller executes the code in the 64K bytes. If the content of application program needs to be modified, the TP2804/TP2804T allows user to activate the In-System Programming (ISP) mode by setting the CHPCON register.

CHPCON (BFH)

| Bit | Name | Function |
|---|---|---|
| 7 | SWRESET | When this bit is and FPROGEN are set to 1, it will enforce microcontroller reset to initial condition just like power on rest. |
| 6 | - | Reserve. |
| 5 | - | Reserve. |
| 4 | ENAUXRAM | 1: Enable on-chip AUX-RAM.<br>0: Disable the on-chip AUX-RAM |
| 3 | - | Reserve |
| 2 | 0 | Must set to 0. |
| 1 | 0 | Must set to 0 |
| 0 | FPROGEN | FLASH EPROM Programming Enable.<br>= 1: enable. The microcontroller enter the in-system programming mode.<br>= 0: disable. The on-chip flash memory is read-only. In-system programmability is disabled. |

ISP_CTRL(E8H)

| Bit | Name | Function |
|---|---|---|
| 7 | ISP_EN | 1:ISP enable |
| 6 | - | Reserve. |
| 5 | - | Reserve. |
| 4 | 1 | Must 1 |
| 3 | 0 | Must 0 |
| 2 | ERASE | Erase bit |
| 1 | Write | Program write into AUX RAM |
| 0 | READ | Read program from AUX RAM |

ISP_ADDR(E9H)

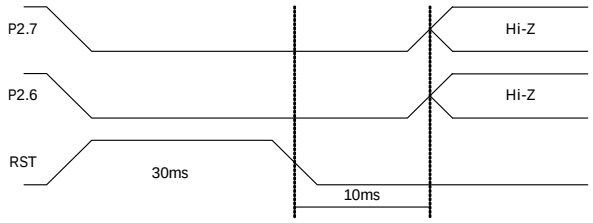
| Bit | Name | Function |
|---|---|---|
| 7 | ADD7 | Address bit 7 |
| 6 | ADD6 | Address bit 6 |
| 5 | ADD5 | Address bit 5 |
| 4 | ADD4 | Address bit 4 |
| 3 | ADD3 | Address bit 3 |
| 2 | ADD2 | Address bit 2 |
| 1 | ADD1 | Address bit 1 |
| 0 | ADD0 | Address bit 0 |

## Hardware Enter ISP MODE

When the reset pin of TP2804/TP2804T is at high level and any of the two conditions described below is fit in.

| P4.3 | P2.7 | P2.6 | Mode |
|---|---|---|---|
| X | L | L | ISP |
| L | X | X | ISP |

**The Reset Timing for Entering ISP Mode**




## Security

During the on-chip FLASH EPROM programming mode, the FLASH EPROM can be programmed and verified repeatedly. Until the code inside the FLASH EPROM is confirmed OK, the code can be protected. The protection of FLASH EPROM and those operations on it are described below.

The TP2804/TP2804T has several Special Setting Registers, including the Security Register that cannot be programmed from low to high. They can only be reset through erases-all operation.

**Special Setting Registers**

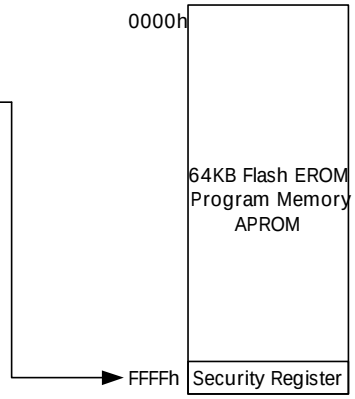
| B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|
| B7 | B6 | B5 | X | X | X | B1 | X |

Security Bits

B1 : Lock bit, logic 0 : active
B5~B7 : Set ISP Address

| B7 | B6 | B5 | Address |
|---|---|---|---|
| 0 | 0 | 0 | F000~FFFF |
| 0 | 0 | 1 | F200~FFFF |
| 0 | 1 | 0 | F400~FFFF |
| 0 | 1 | 1 | F600~FFFF |
| 1 | 0 | 0 | F800~FFFF |
| 1 | 0 | 1 | FA00~FFFF |
| 1 | 1 | 0 | FC00~FFFF |
| 1 | 1 | 1 | FE00~FFFF |

X : Reserved




## Lock bit

This bit is used to protect the customer's program code in the TP2804/TP2804T. It may be set after the programmer finishes the programming and verifies the sequence. Once this bit is set to logic 0, both the Flash EROM data and Setting Registers cannot be accessed again.

## Absolute Maximum Ratings

($V_{DD}$-$V_{SS}$ = 5V ±10% for TP2804H/TP2804TH, $V_{DD}$-$V_{SS}$ = 3.3V ±10% for TP2804L)

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| DC Power Supply | $V_{DD}$-$V_{SS}$ | -0.3 | $V_{DD}$+1 | V |
| Input Voltage | $V_{IN}$ | $V_{SS}$-0.3 | $V_{DD}$+0.3 | V |
| Operation Temperature | $T_A$ | 0 | 70 | ˚C |
| Storage Temperature | $T_{ST}$ | -55 | +150 | ˚C |

NOTE: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

## DC Electrical Characteristics

($V_{DD}$-$V_{SS}$ = 5V ±10% for TP2804H/TP2804TH, $V_{DD}$-$V_{SS}$ = 3.3V ±10% for TP2804L, $T_A$ = 25˚C, Fosc = 12MHz, unless otherwise specified)

| Parameter | Symbol | Min | Max | Unit | Test Condition |
|---|---|---|---|---|---|
| Operating Voltage | $V_{DD}$ | 0.9 $V_{DD}$ | 1.1 $V_{DD}$ | V | RST = 1, P0 = $V_{DD}$ |
| Operating Current | $I_{DD}$ | - | 20/8 | mA | No load, $V_{DD}$ = 5V/3.3V |
| Idle Current | $I_{IDLE}$ | - | 6/3 | mA | Idle mode, $V_{DD}$ = 5V/3.3V |
| Power Down Current | $I_{PWDN}$ | - | 100 | μA | Power-down mode, $V_{DD}$ = 5V/3.3V |
| Input Current P1, P2, P3, P4 | $I_{IN1}$ | -50 | +10 | μA | $V_{IN}$ = 0V or $V_{DD}$ |
| Input Current RST | $I_{IN2}$ | -10 | +300 | μA | 0＜$V_{IN}$＜$V_{DD}$ |
| Reset Threshold [*5] | $V_{POR}$ | 3.9 | 4.0 | V | $V_{DD}$ |
| Input Low Voltage P0, P1, P3, P4, $\overline{EA}$ | $V_{IL1}$ | 0 | 0.2$V_{DD}$–0.2 | V | $V_{DD}$ |
| Input Low Voltage RST | $V_{IL2}$ | 0 | 0.2$V_{DD}$–0.2 | V | $V_{DD}$ |
| Input Low Voltage XTAL1 [*4] | $V_{IL3}$ | 0 | 0.2$V_{DD}$–0.3 | V | $V_{DD}$ |
| Output Low Voltage P1, P2, P3, P4, $\overline{EA}$ | $V_{IH1}$ | 3.5/2.6 | $V_{DD}$+0.2 | V | $V_{DD}$ = 5.5V/3.3V |
| Input High Voltage RST | $V_{IH2}$ | 3.5/2.6 | $V_{DD}$+0.2 | V | $V_{DD}$ = 5.5V/3.3V |
| Input High Voltage XTAL1 [*4] | $V_{IH3}$ | 3.5/2.6 | $V_{DD}$+0.2 | V | $V_{DD}$ = 5.5V/3.3V |
| Output Low Voltage P1, P2, P3, P4 | $V_{OL1}$ | - | 0.45 | V | $V_{DD}$ = 5V/3.3V $I_{OL}$ = +2mA |
| Output Low Voltage P0 , ALE, PSEN [*3] | $V_{OL}$2 | - | 0.45 | V | $V_{DD}$ = 5V/3.3V, $I_{OL}$ = +4mA |
| Sink Current P1, P3, P4 | $I_{SK1}$ | - | 8/6 | mA | $V_{DD}$ = 5V/3.3V, $V_{IN}$ = -0.45V |
| Sink Current P0, P2, ALE, PSEN | $I_{SK2}$ | - | 8/6 | mA | $V_{DD}$ = 5V/3.3V, $V_{IN}$ = 0.45V |
| Output Low Voltage P1, P2, P3, P4 | $V_{OH1}$ | 2.4/2.0 | - | V | $V_{DD}$ = 5V/3.3V |
| Output High Voltage P0 , ALE, PSEN [*3] | $V_{OH2}$ | 2.4/2.0 | - | V | $V_{DD}$ = 5V/3.3V |
| Source Current P0, P2, P3, P4 | $I_{Sr1}$ | -120/-80 | -200/-120 | μA | $V_{DD}$ = 5V/3.3V, $V_{IN}$ = 2.4V |

NOTES:

1. RST pin is an Schmitt trigger input.
2. P0, ALE and /PSEN are tested in the external access mode.

*3. XTAL1 is a CMOS input.

*4. Pins of P1, P2, P3 and P4 can source a transition current when they are being externally driven 1 to 0. The transition current reaches its maximum value when $V_{IN}$ approximates to 2V.

*5. TP2804T only. It asserts a reset signal whenever the VDD supply voltage declines below $V_{POR}$.

## AC Electrical Characteristics

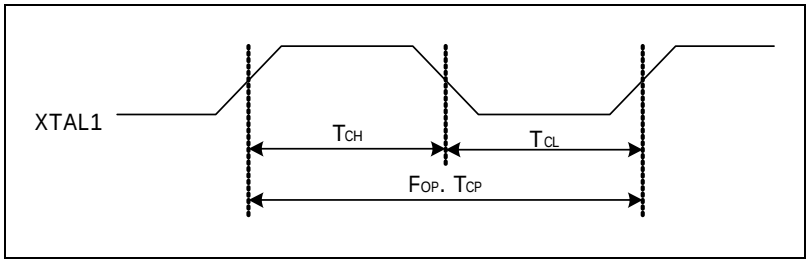
The AC specifications are a function of the particular process used to manufacture the part, the ratings of the I/O buffers, the capacitive load, and the internal routing capacitance. Most of the specifications can be expressed in terms of multiple input clock periods ($T_{CP}$), and actual parts will usually experience less than a ±20 nS variation. The numbers below represent the performance expected from a 0.6 micron CMOS process when using 2 and 4 mA output buffers.

| Parameter | Symbol | Min | Max | Unit | Test Conditions |
|---|---|---|---|---|---|
| Operating Speed | $F_{OP}$ | 0 | 40 | MHz | 1 |
| Clock Period | $T_{CP}$ | 25 | - | nS | 2 |
| Clock High | $T_{CH}$ | 10 | - | nS | 3 |
| Clock Low | $T_{CL}$ | 10 | - | nS | 3 |
| Power-on-reset assert | $T_{POR}$ | 140 | 400 | mS | 4 |

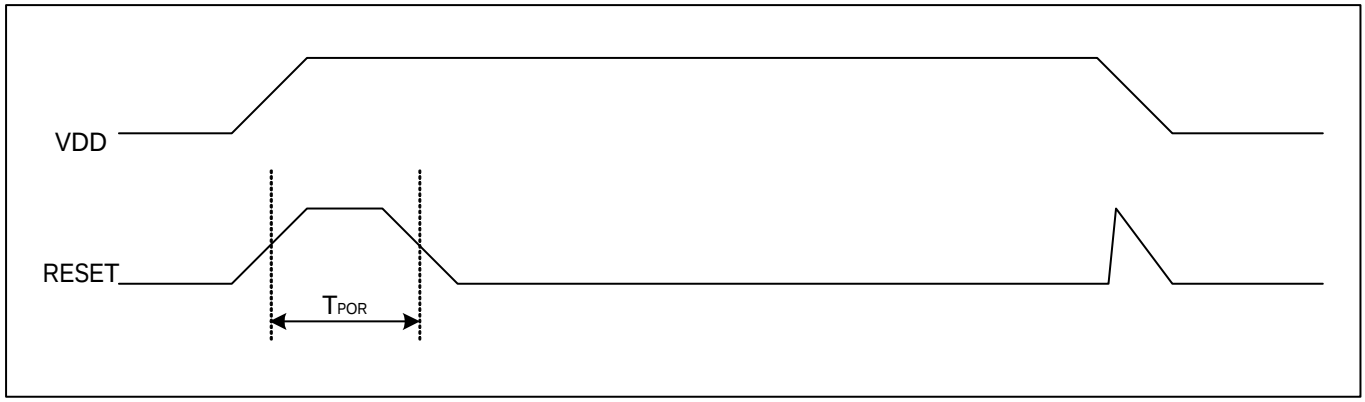
NOTES:

1. The clock may be stopped indefinitely in either state.
2. The $T_{CP}$ specification is used as a reference in other specifications.
3. There are no duty cycle requirements on the XTAL 1 input.
4. The assert RESET whenever VDD supply voltage declines under 4V

## Clock Input Waveform




## Power-on-reset Wafeform



## Data Read Cycle

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| ALE Low to /RD Low | $T_{DAR}$ | 3 $T_{CP}$-△ | - | -3 $T_{CP}$+△ | nS | 1, 2 |
| /RD Low to Data Valid | $T_{DDA}$ | - | - | 4 $T_{CP}$ | nS | 1 |
| Data Hold from /RD High | $T_{DDH}$ | 0 | - | 2 $T_{CP}$ | nS | |
| Data Float from /RD High | $T_{DDZ}$ | 0 | - | 2 $T_{CP}$ | nS | |
| /RD Pulse Width | $T_{DRD}$ | 6 $T_{CP}$-△ | 6 $T_{CP}$ | - | nS | 2 |

NOTES:

1. Data memory access time is 8 $T_{CP}$.
2. 〝△〞（due to buffer driving delay and wire loading ）is 20 nS.

## Data Write Cycle

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| ALE Low /WR Low | $T_{DAW}$ | 3 $T_{CP}$-△ | - | 3 $T_{CP}$ | nS |
| Data Valid to /WR Low | $T_{DAD}$ | 1 $T_{CP}$-△ | - | - | nS |
| Data Hold from /WR High | $T_{DWD}$ | 1 $T_{CP}$-△ | - | - | nS |
| /WR Pulse Width | $T_{DWR}$ | 6 $T_{CP}$-△ | 6 $T_{CP}$ | - | nS |

NOTE: 〝△〞（due to buffer driving delay and wire loading ）is 20 nS.

## Port Access Cycle

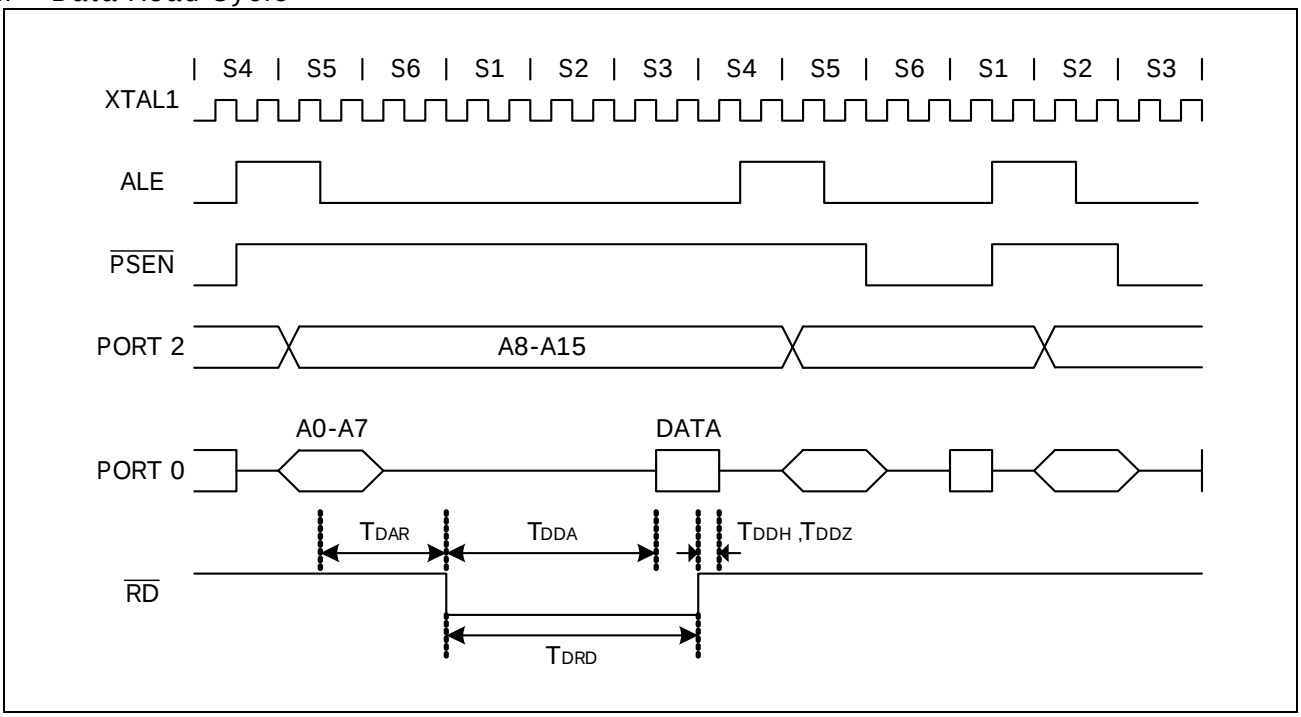
| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Port Input Setup to ALE Low | $T_{PDS}$ | 1 $T_{CP}$ | - | - | nS |
| Port Input Hold from ALE Low | $T_{PDH}$ | 0 | - | - | nS |
| Port Output to ALE | $T_{PDA}$ | 1 $T_{CP}$ | - | - | nS |

NOTES:

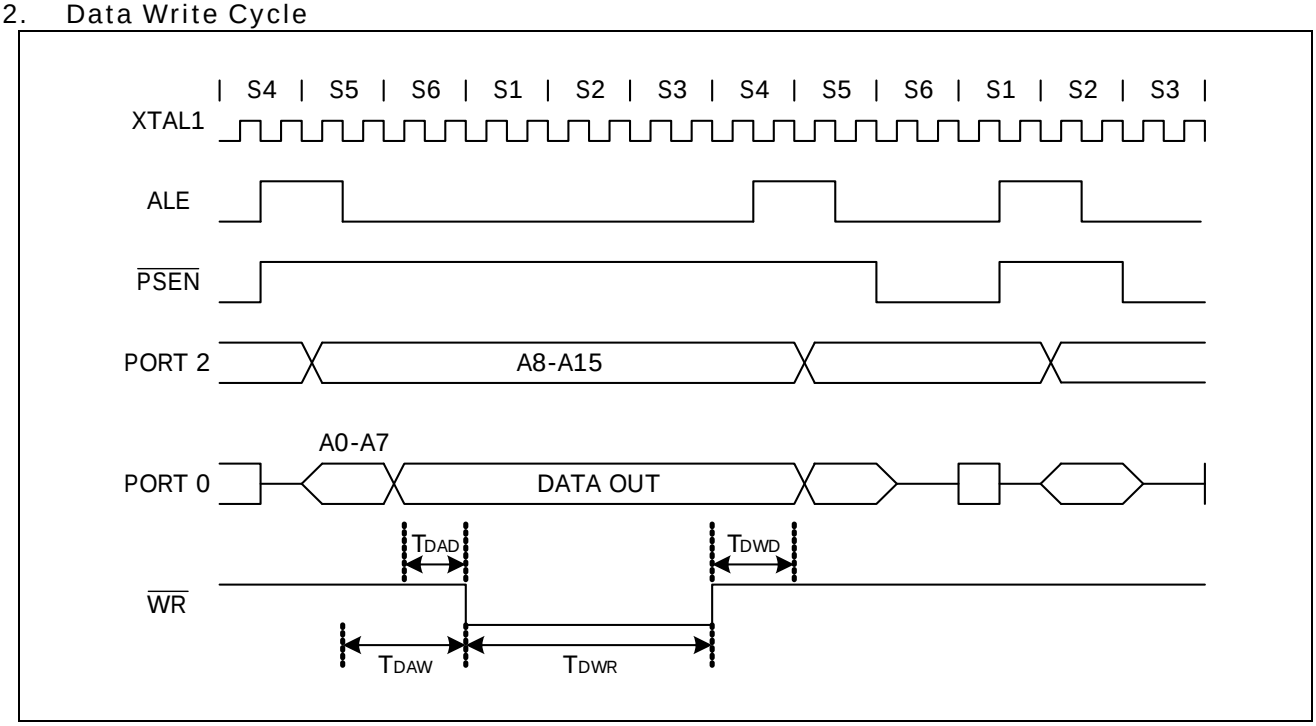
1. Ports are read during S5P2, and output data becomes available at the end of S6P2.
2. The timing data are referenced to ALE, since it provides a convenient reference.

## Timing Waveforms

### 1. Data Read Cycle

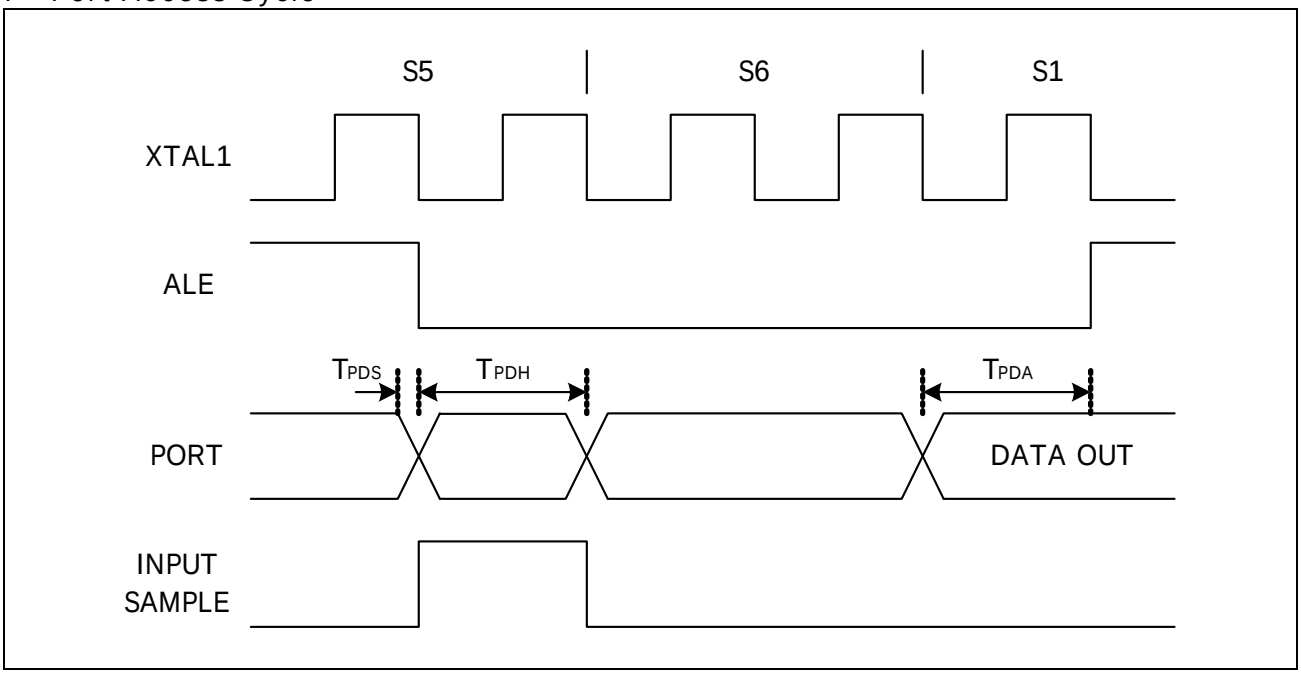


2. Data Write Cycle




## Timing Waveforms (continued)

3. Port Access Cycle



## Application Diagrams

### 1. Internal Program, Memory and Crystal

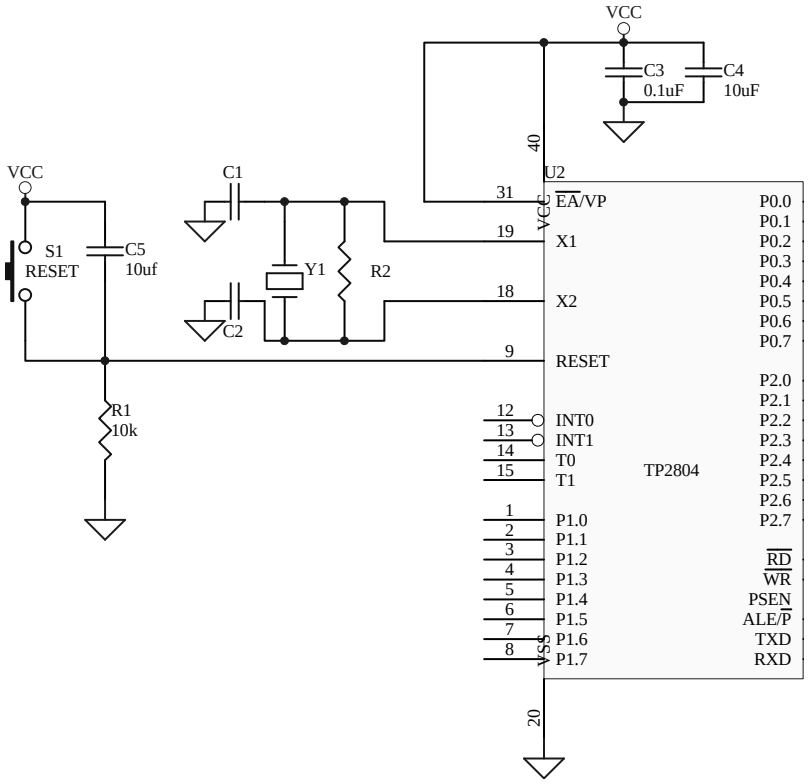



Figure A

| CRYSTAL | C1 | C2 | R2 |
|---|---|---|---|
| 6MHz | 47P | 47P | - |
| 16MHz | 30P | 30P | - |
| 24MHz | 15P | 15P | - |
| 32MHz | 10P | 10P | 6.8K |
| 40MHz | 5P | 5P | 4.7K |

NOTE: Above table shows the reference values for crystal applications.

Note: For TP2804T the external RC reset circuit can be removed.

## 2. Expanded External Program and Data Memory and Oscillator

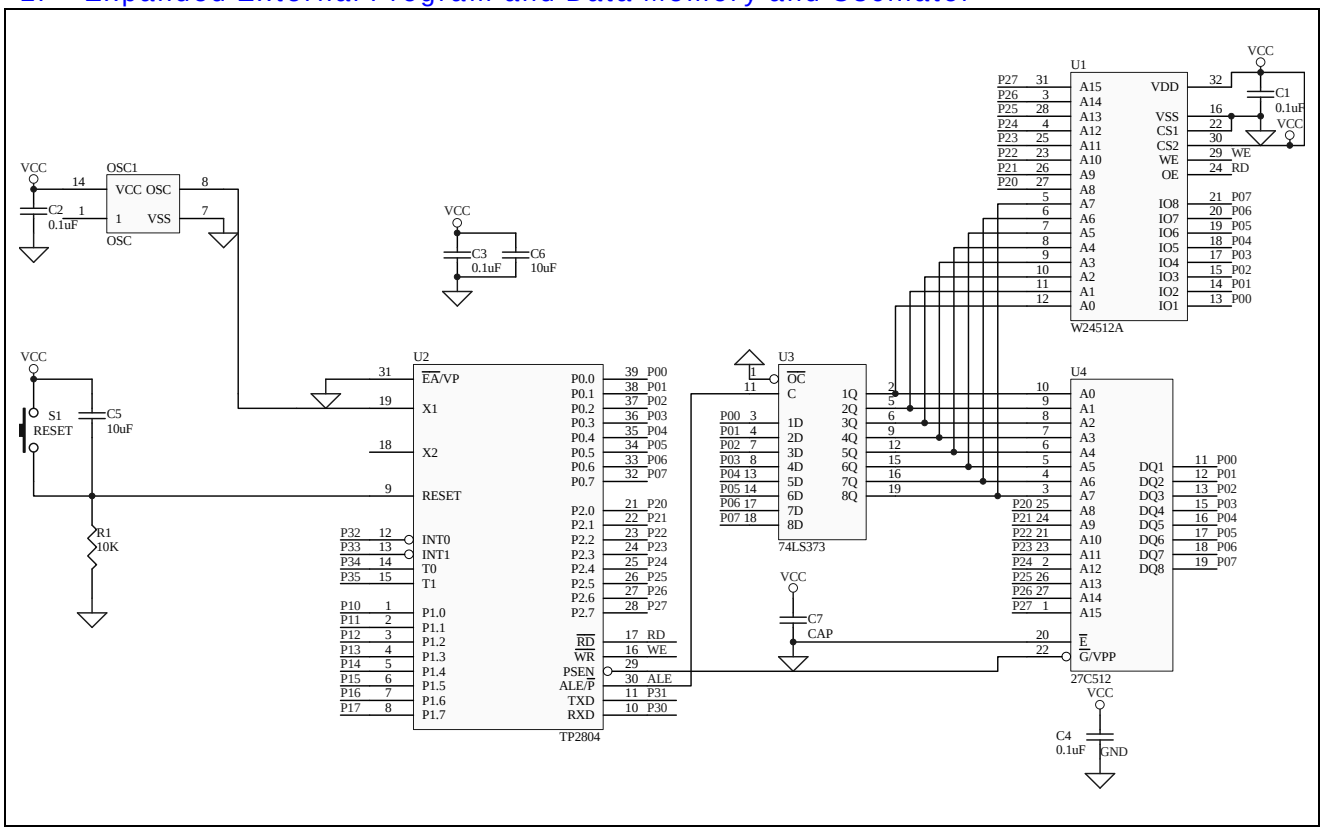
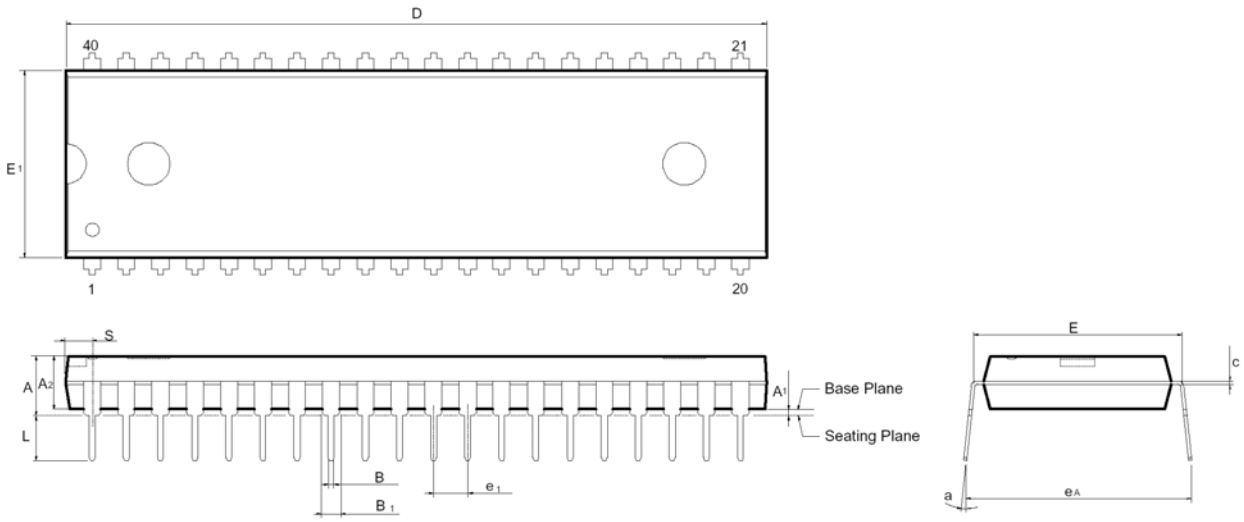



Figure B

Note: For TP2804T the external RC reset circuit can be removed.

## Package Information

### 40-pin DIP



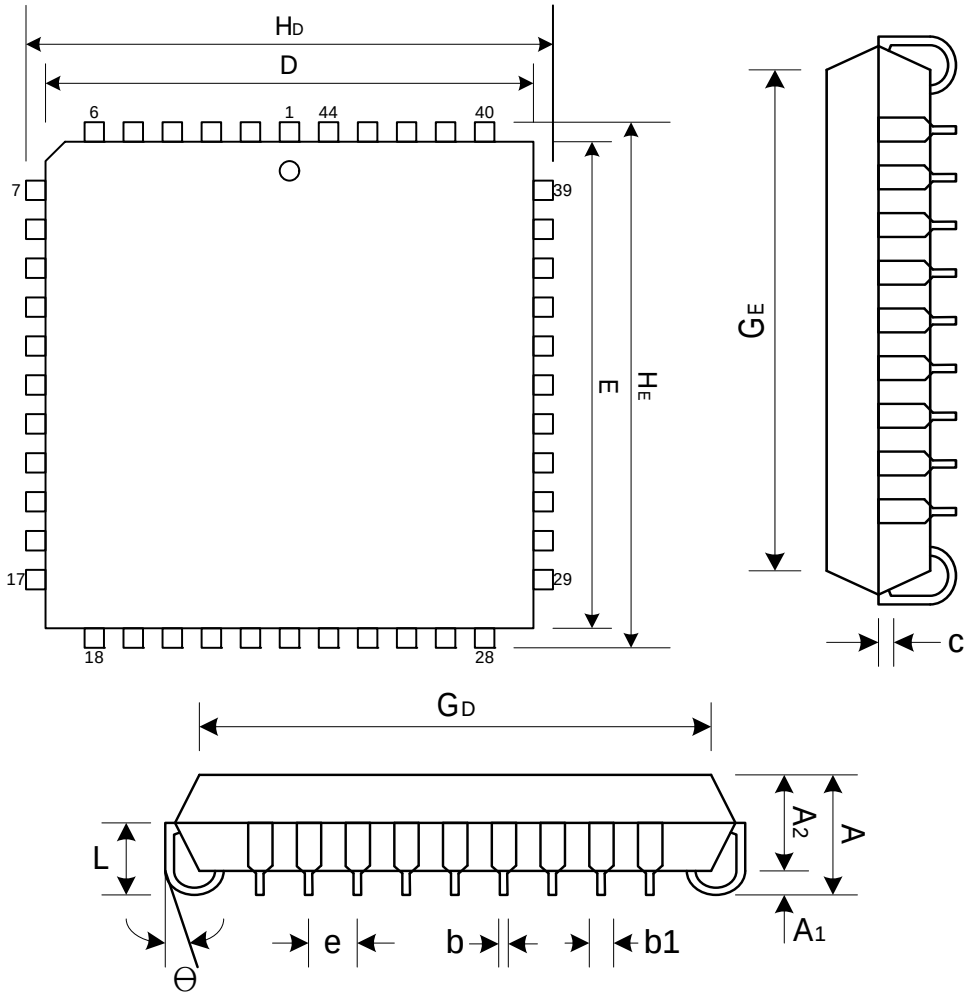

Unit: Millimeter

| Symbol | Dimension in mm | | |
|---|---|---|---|
| | Min. | Nom. | Max. |
| A | — | — | 5.588 |
| A1 | 0.381 | — | — |
| A2 | 3.81 | 3.937 | 4.064 |
| B | — | 0.457 | — |
| B1 | — | 1.27 | — |
| D | 52.197 | 52.324 | 52.578 |
| E | 15.24 BSC | | |
| E1 | 13.716 | 13.843 | 13.97 |
| e1 | — | 2.54 | — |
| L | 2.921 | 3.302 | 3.81 |
| a | 0 | 177.8 | 381 |
| eA | 16.002 | 16.51 | 17.018 |

NOTES:

1. Dimension D Max. includes mold flash or tie bar burrs.
2. Dimension E1 does not include interlead flash.
3. Dimensions D and E1 include mold mismatch and are determined at the mold parting line.
4. Dimension B1 does not include dam bar protrusion/intrusion.
5. JEDEC Outline: MS-011 AC

## 44-pin PLCC



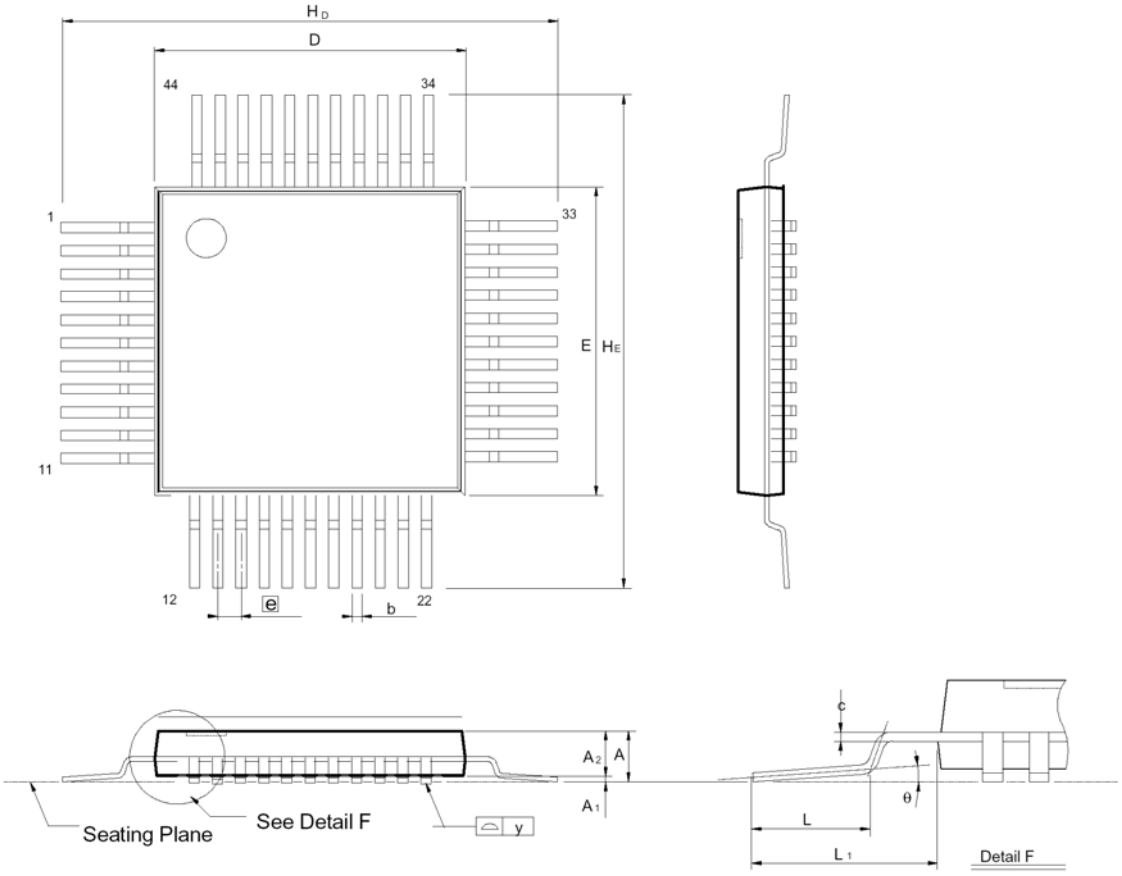

Unit: Millimeter

| Symbol | Dimension in mm | | |
|---|---|---|---|
| | Min. | Nom. | Max. |
| A | — | — | 4.699 |
| A1 | 0.508 | — | — |
| A2 | 3.683 | 3.81 | 3.937 |
| b1 | 0.6604 | 0.7112 | 0.8128 |
| b | 0.4064 | 0.4572 | 0.5588 |
| c | 0.1778 | 0.254 | 0.3302 |
| D | 16.4592 | 16.5862 | 16.7132 |
| E | 16.4592 | 16.5862 | 16.7132 |
| e | 1.27 BSC | | |
| $G_D$ | 14.986 | 15.494 | 16.002 |
| $G_E$ | 14.986 | 15.494 | 16.002 |
| $H_D$ | 17.272 | 17.526 | 17.78 |
| $H_E$ | 17.272 | 17.526 | 17.78 |
| L | 2.286 | 2.54 | 2.794 |

NOTES:

1. Dimensions D and E do not include interlead flash and mold protrusion. Allowable protrusion is 10 mil per side.
2. Dimension b1 does not include dam bar protrusion/intrusion.
3. JEDEC Outline: M0-047 AC.

## 44-pin PQFP




Unit: Millimeter

| Symbol | Dimension in mm | | |
|---|---|---|---|
| | Min. | Nom. | Max. |
| A | — | — | 2.7 |
| A1 | 0.25 | — | 0.5 |
| A2 | 1.9 | 2.0 | 2.2 |
| b | | 0.3 TYP. | |
| c | 0.10 | 0.15 | 0.20 |
| D | 9.9 | 10.00 | 10.1 |
| E | 9.9 | 10.00 | 10.1 |
| e | | 0.80 TYP. | |
| $H_D$ | 13 | 13.2 | 13.4 |
| $H_E$ | 13 | 13.2 | 13.4 |
| L | 0.73 | 0.88 | 0.93 |
| L1 | — | 1.6 | — |
| y | | 0.10 | |
| $\theta^\circ$ | 0° | — | 7° |

NOTES:

1. Dimensions D and E do not include interlead flash.
2. Dimension b does not include dam bar protrusion/intrusion.
3. JEDEC Outline: MO-108 AA-1.